

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 0: Welcome

Sammy Kayali

Advanced Microprocessor Radiation Testing Technical Peer Review

•The Remote Engineering and Exploration (REE) Project is evaluating the use of advanced commercial microprocessors for on-board data processing in spacecraft. One of the project's main thrusts has been radiation testing of the Power PC750 microprocessor, a high-performance processor with power dissipation of 6 Watts.

•The purpose of this review is to provide a critique of the results of the work completed at this point, along with the proposed direction of subsequent work planned for this fiscal year.

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Key Objectives of the Peer Review

- Convene a group of qualified experts to review progress, technical quality, objectives and future direction for the study.
- Evaluate specific findings of the study, including the following areas:
 - (a) Test techniques and methods used for testing these complex devices
 - (b) Specific test results and data analysis methods
 - (c) Validity of the test results and methods of estimating error rates in space
- Provide a formal critique of the work that represents the consensus view of the review panel.
- Assess the feasibility of using acquired experimental test data in the development of effective fault tolerance methods and tools.

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Requested Outputs

- Individual responses to evaluation form.
- Brief consensus summary report by the committee, coordinated by E-mail.
- Specific comments from individual review board members, as deemed necessary.

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Outline

Overview of the REE Program	Rafi Some
Background	Allan Johnston
Test Approach	Gary Swift
Proton Test Results	Doug Millward
Test Methods	Gary Swift
Data Analysis Methods	Doug Millward
Heavy Ion Test Results	Steve Guertin
Proton/Heavy Ion Results Comparison	Larry Edmonds
Space Environments	Allan Johnston
REE Fault Model Overview	Arbi Karapetian
Error Rate Calculation	Larry Edmonds
Error Rate Results	Gary Swift
Conclusion and Near-Term Plans	Gary Swift

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Rafi Some

Project Scientist: James C. Ling

- REE is a technology project funded by NASA Code S for developing an onboard supercomputing capability for space applications.
- REE is one of five projects under the NASA HPPC Program. The other four projects are:
 - CAS - Computational Aerospace Sciences
 - ESS - Earth and Space Sciences
 - LT - Learning Technologies and
 - NREN - NASA Research and Educational Network
- The goal of REE is to use the state of the art commercial-of-the-shelf computer technology in space to significantly enhance the scientific objectives of the mission at a greatly reduced cost.
- REE will achieve onboard computing capability of >300 MOPS/watt scalable to mission requirements. The current RAD6000 (the state of the art radiation hardened microprocessor) single board computer operates at ~ 1 MOPS/watt.

NREN (NASA Research and Educational Network): Extend U.S. technological leadership in computer communications through research and development that advances leading edge networking technology and services, then apply these enhanced capabilities to NASA mission and educational services.

Rad-hard components are always at least 2 generations behind commercial State Of The Art

Legend:

- new (solid circle)
- Motorola 68010 (open circle)
- PowerPC (solid square)
- Microns (solid diamond)

Component / System	Launch Year	Reliability
88020/32	1987	12
88030/50	1988	15
88040/40	1989	25
88040/75	1989	20
88040/75	1990	10
88040/75	1991	20
88040/75	1992	20
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88		

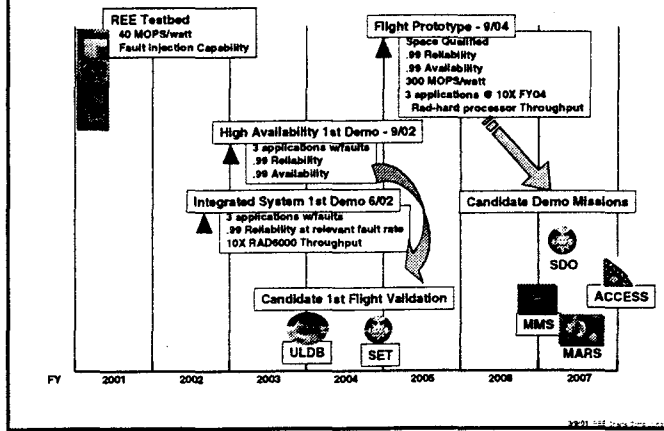
- **Viability of COTS Hardware for Space Missions**
 - **Commercial Technology Family viability prediction**
 - Characterizing commercial component technologies with respect to radiation hardness and susceptibility to single event effects to a level that allows modeling and prediction of their behavior in a space environment without exhaustive testing
 - **Low cost hardware solutions to mitigating single event effects and attain mission life reliability**
 - Memory organization, watchdog timers, fault tolerant controllers and interfaces for assembling COTS boards into a system
 - **Low cost packaging and assembly methods for dealing with launch/landing shock & vibration, and in-space thermal management**
 - Commercial components assume a convection cooling environment

REE Critical Technology Development

- Software Methods for maintaining system reliability and availability in the presence of random transient errors and permanent faults
 - Highly reliable system level error detection and recovery
 - Software layer to detect hardware, operating system, and application process failures, and reliably recover to a functioning system state
 - Low overhead applications error detection and recovery
 - Application specific error detection methods that do not require replication of the computation
 - Fast recovery methods for restoring correct applications state
- Space Radiation Environment Effects Simulation Capability
 - Random transient error injection that replicates the errors predicted by the space environment models and can be tailored to specific mission orbits or trajectories
 - System monitoring functions that allow the observation of the effects of transient errors on software

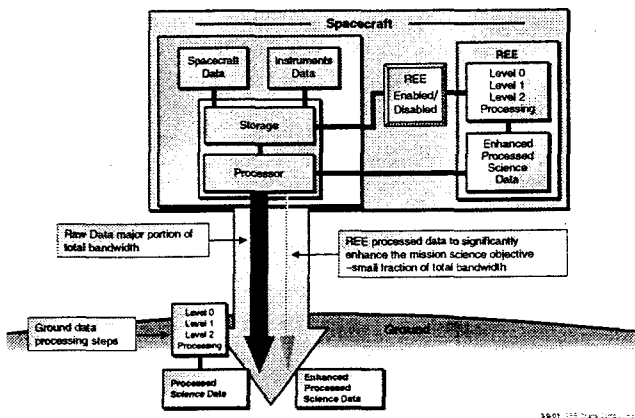
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REE Major Milestones (replan)



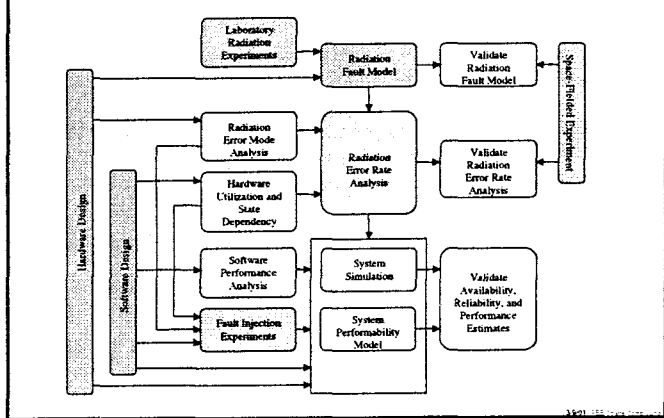
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REE Demonstration Flight Applications



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Methodology Overview



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REE Two-Level Architecture

PROCESSING
ELEMENT
(PE)

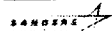
- Processing Element - Direct Use Of COTS For Maximum System Impact**
- Highest performance-power based on latest commodity microprocessors
 - Direct leverage of COTS software investments
 - Specific processor and OS candidates are independent of core architecture

NODE
CONTROLLER
(NC)

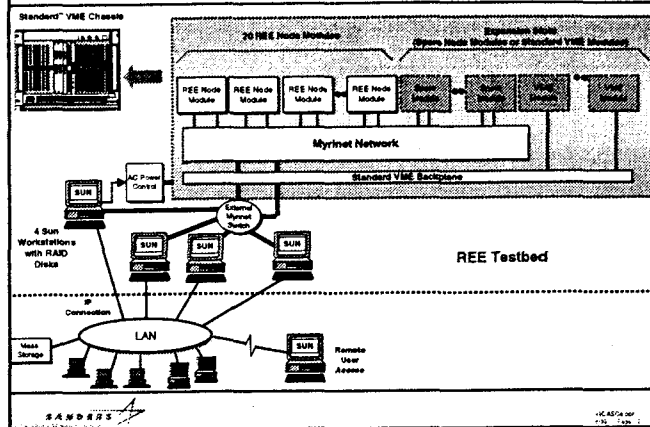
- Node Controller - Enables Rapid Technology Insertion Cycles**
- Open architecture, technology neutral interfaces
 - Provides reliable control and communications to REE systems
 - Low power design for "system on a chip" integration for space flight transition

NETWORK
FABRIC

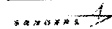
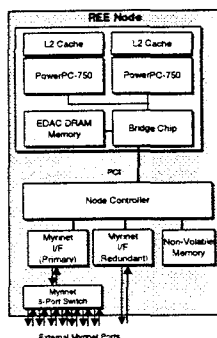
- Scalable Network**
- COTS standard network with long technology life cycle
 - Scalable, high bandwidth for supercomputer application
 - Fault resilient to enable reliable space system application

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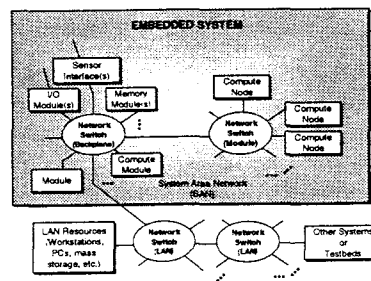
REE First Generation Testbed

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REE Node Architecture

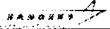
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Myrinet Scalable Network



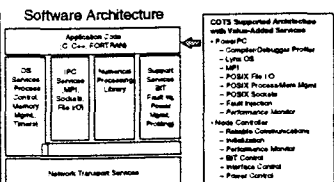
Myrinet Technology

- Full-duplex 1.28+1.28 Gbit/sec links
- Low-latency cut-through multi-stage switches
- Flexible topology support
- Maximum limit of 64,000 nodes
- Self-configuring support
- Variable packet length
- Message protocol neutral
- Packet CRC at each link
- Low-voltage interfaces
- Future upgrade to 2x bandwidth

MCAP-01-01
1-95-1-1-1-1

REE Software Architecture

Proven method for seamless code portability between workstation and testbed. Communications uses low power node controller to maximize performance per watt. Reliable communications layer enhances fault tolerance and provides the foundation for SIFT. Standards-based approach preserves investment for future flight use. COTS-based operating system, development tools, and hardware leverage commercial investments. Value-added services for fault injection, power control and monitoring, system configuration, logging, provide a robust environment for SIFT experimentation.

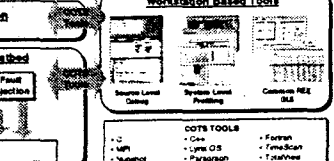


Step 1: Algorithm development and analysis

Step 2: Algorithm timing, power consumption and super-resolution/visualization

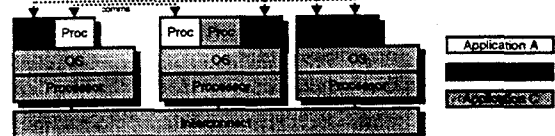
Step 3: Algorithm re-optimization and re-partitionization super-optimization

Step 4: Algorithm fault detection, isolation, and recovery experimentation

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REE Testbed Programming Model

- REE Programming Model is a Distributed System with Message Passing:
 - An independent operating system per processor
 - Multiple processes per processor, both user level and supervisory level
 - All supervisory level processes (threads) share the same address space
 - All user process have separate, protected address spaces
 - Multi-threading of both user and supervisory processes is fully supported
 - Multiple processes per processor. Processes can control other processes.
 - Applications consist of one or more processes that communicate among themselves
 - Within a processor, communications is through either shared memory or message passing
 - Between processors, communications is through message passing



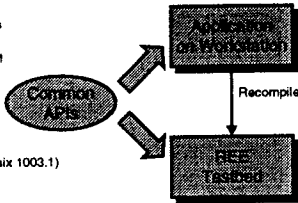
Accepted programming paradigm supports general purpose computing.

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Portable Application Programming Interfaces

• Portable Application Programming Interfaces:

- MPI 1.2
 - Subset chosen for best value
 - Support multi-threaded processes
 - Support multiple independent processes
 - C, C++, and Fortran bindings
 - Demonstrate MPI-IO subset built on MPI
- COTS OS
 - Standard Unix File I/O
 - Threads (Posix 1003.1c)
 - Sockets (Posix 1003.1g)
 - NFS and RPC
 - Process and Memory Management (Posix 1003.1)
 - Posix 1003.1b real-time extensions
- Numerical Processing Library (COTS)



Standards-based APIs facilitate the portability of applications

Following Charts Were Not On The DASC Paper

Node Controller Hardware Fault Tolerance Support

NC Processor support

- Illegal instruction interrupt
- Memory management unit
- System bus timeout watchdog
- Memory/PCI access protection
- Memory parity detection
- Sector CRC check on external NVM (SW)
- Watchdog timers

BIT control, health and status support facilities

- Facility for BIT control, fault logging, and reporting for node
- Facility for primary-redundant network interface enable and power control

PCI support

- Parity error
- System error
- Terminate and violation
- Access violation

NTE support

- Parameter Table RAM parity check
- Message level CRC check and reporting

Myrinet fabric I/F support

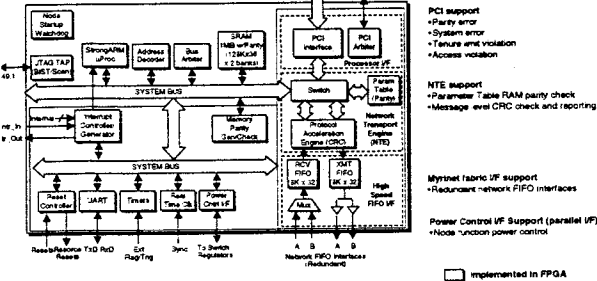
- Redundant network RIFO interfaces

Power Control I/F Support (parallel I/F)

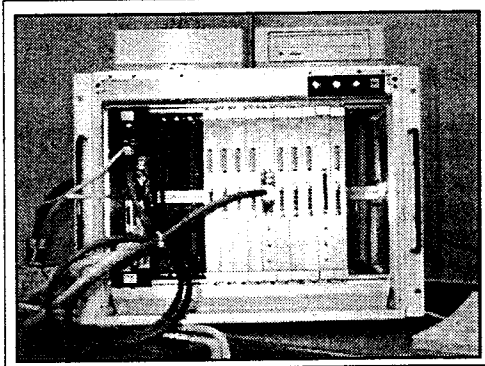
- Node function power control

implemented in FPGA

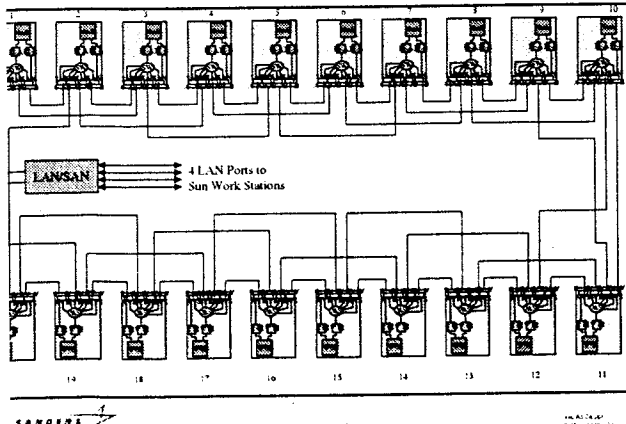
de startup support
PGA load time out
voltage/temperature time out
no node restart / shutdown



Standard VME Chassis



REE Testbed Configuration

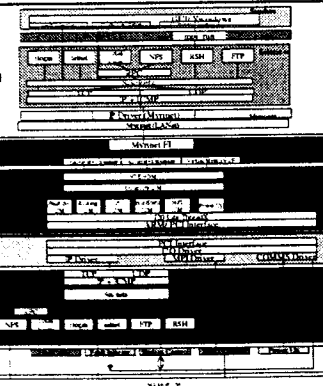


REE Software Architecture

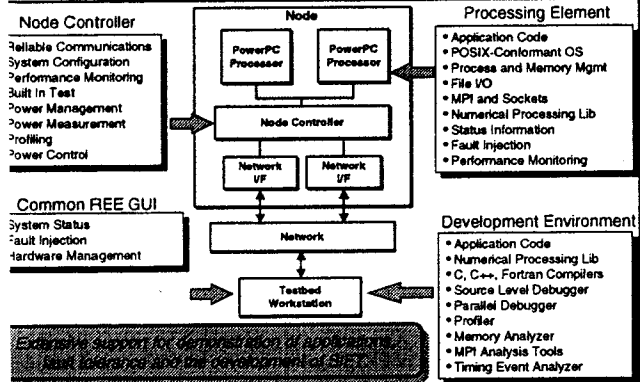
Sun workstation

Node Controller

PPC 750



The REE Software Architecture



Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 2: Background

Allan Johnston

Outline

Earlier Approaches for Microprocessor Testing

- Register tests
- Application software
- "Golden" chip
- Watchdog timer to define hangs and crashes

General Testing Issues

- Operational conditions
- Error latency

Practical Testing Issues

- Flip-chip construction
- Power dissipation

Earlier Test Results

General Scaling Issues

2

Earlier Testing Approaches

Register-Level Testing

- Reduces results to familiar terms
- May be extended to real applications
- Doesn't adequately test microprocessor core

Application Software

- Difficult to extend to other applications
- Results highly variable

Golden Chip

- Lockstep comparison
- Provides clock-cycle error visibility

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Operating Systems

Machine Language

- No operating system
- Software development and monitoring difficult for advanced devices

Board-Level Operating System

- Primitive with minimum overhead
- Provides I/O, status and easy interfacing

Higher-Level Operating Systems

- Extremely complex
- Mask processor activity
- Very limited internal visibility

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RAD6000 Processor

Version 0

- Hardened for total dose, but not for single-event upset
- SEU data on Version 1 from manufacturer used to calculate upset rates for Pathfinder

Version 1

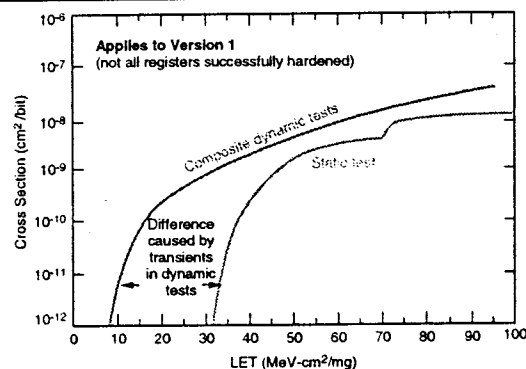
- This version flown on Pathfinder
- Hardened for single-event upset
 - Several internal registers were overlooked
 - Intermediate SEU hardness
 - One possible error in 9-month mission ("quiet" period)

Version 2

- Fixed oversights in Version 1
- Advertised register error rate 5.3×10^{-9} errors per bit-day

5

Radiation Test Results for RAD6000



Augmentation of Register-Level Testing

Status Monitoring

- Provides additional visibility
- Easily implemented

Adding Additional Processor Functions

- Cache
- Floating point operations

Watchdog Timer

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Practical Testing Issues

Flip-Chip Bonding

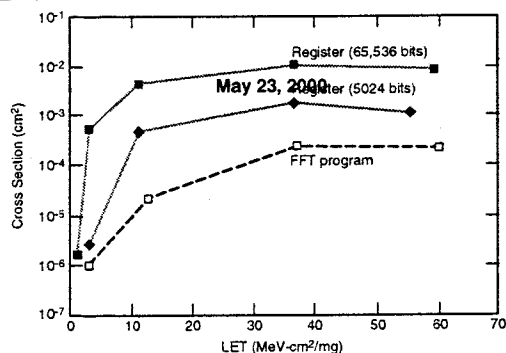
- Eliminates ability to "delid" device
- SEU testing still possible with extremely energetic ions
- Back irradiation provides an alternative approach
 - Mechanical "thinning" reduces range requirement
 - May not be equivalent to top irradiation
 - Thinning may alter device properties

Power Dissipation

- Power PC750 dissipates 6W at full speed
- Difficult issue in vacuum chamber
- Heating may be worse for thinned samples

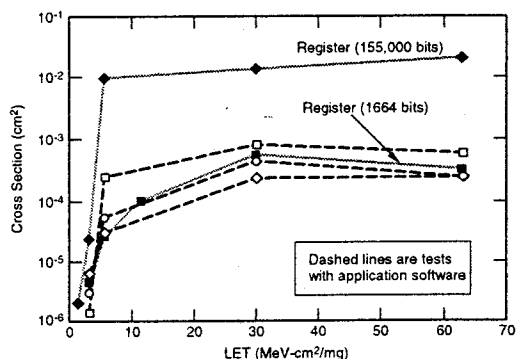
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Single-Event Upset Results for PC603e



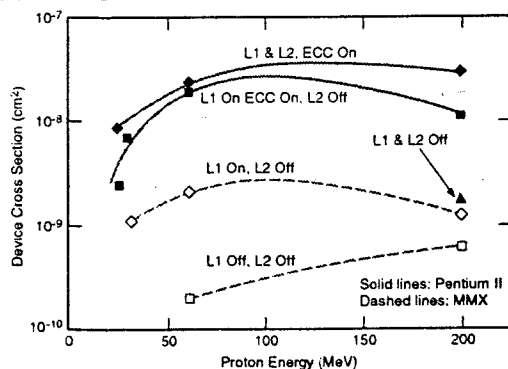
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Single-Event Upset Results for Intel 486



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Proton Upset Results for Advanced Intel Processors



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Intel Processor Tests

Intended for Space Station Application

- Dominated by protons (no heavy ion testing done)
- Used high-level operating system

Two types of software

- DOS-based program
- NT-based program

Operating System "Crashes" Dominated

- Register error not observed in many of the runs
- Results difficult to compare with more basic tests

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Other Considerations

Newer Processors Are More Complex

- Larger number of registers
- Cache memory nearly always used
- Increases *chip* error rate

Processors "Crash" Frequently During Radiation Testing

- Many possible operational failures
- Nearly impossible to categorize
- Crashes in applications may be difficult to deal with
 - Identification and latency
 - Recovery modes

Crashes Very Infrequent in Hardened Processors

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Dealing with "Hangs"

"Hangs" Interfere with Error Rate Measurements

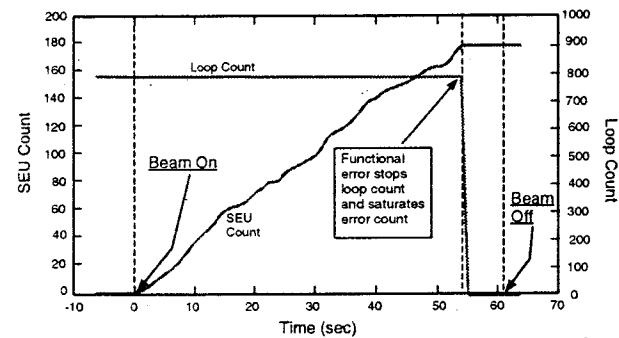
- Affect statistical uncertainty of measurements
- Difficult to categorize

Ways to Minimize Effect of "Hangs"

- Use very simple test algorithms
- Validate partial runs

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"Strip Chart" Approach for Error Recognition



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Other Considerations

SEU Rates in Commercial Processors Are Not Controlled

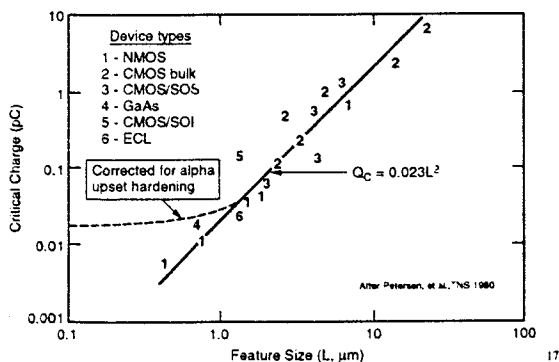
- SEU sensitivity and upset rate may change with manufacturing improvements (not a factor for hardened processors)
- Frequent testing required for critical applications

Commercial Processors Appear Satisfactory for Non-Critical Data Processing

- Substantial risk if used for spacecraft control or critical data
- Error rates unacceptable during solar flares
- Processor crashes not thoroughly characterized
- Spacecraft control generally does not need processing speed of advanced devices

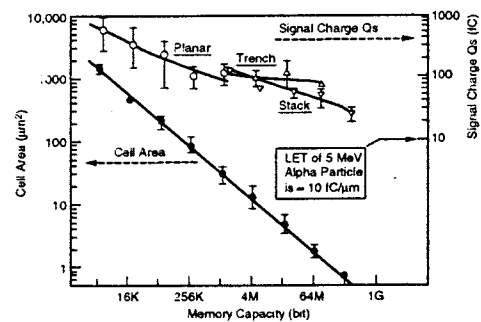
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Device Scaling: Early Results by Petersen, et al.



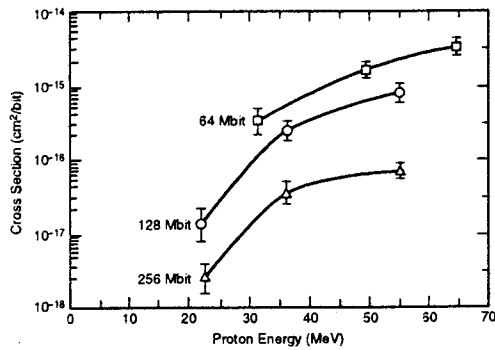
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DRAM Scaling: Basic Design



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DRAM Scaling: Proton Upset



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Scaling Trends (after Davari)

Parameter	Late 1980's	1992	1995	1998	2001	2004
Supply voltage (V)	5	5/3.3	3.3/2.5	2.5/1.8	1.5	1.2
High performance	-	3.3/2.5	2.5/1.5	1.5/1.2	1.0	1.0
Low power	-	-	-	-	-	-
Lithog. resolution (μm)	1.25	0.8	0.5	0.35	0.25	0.18
Channel length (μm)	0.9	0.6/0.45	0.35/0.25	0.2/0.15	0.1	0.07
Gate oxide thickness (nm)	23	15/12	9/7	6/5	3.5	2.5
Relative density	1.0	2.5	6.3	12.8	25	48
Relative speed	1.0	1.4/2.0	2.7/3.4	4.2/5.1	7.2	9.6
High performance	-	1.0/1.6	2.0/2.4	3.2/3.5	4.5	7.2
Low power	-	-	-	-	-	-

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Microprocessor Scaling

Device	Manuf.	Year	Feature Size (approx.)	Threshold LET (MeV-cm²/mg)
Z-80	Zilog	1986	3 μm	1.5 - 2.5
8086	Intel	1986	1.5 μm	1.5 - 2.5
80386	Intel	1991	0.8 μm	2 - 3
68020	Mot.	1992	0.8 μm	1.5 - 2.5
LS64811	LSI	1993	1.2 μm	2 - 2.5
90C601	MHS	1993	1.2 μm	2 - 2.5
80386	Intel	1996	0.6 μm	2 - 3
PC603e	Mot.	1997	0.4 μm	1.7 - 3
Pentium	Intel	1997	0.35 μm	2 - 3
Power PC750	Mot.	2000	0.25 μm	2 - 2.5

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Scaling for Microprocessors

Complex Problem with Several Competing Factors

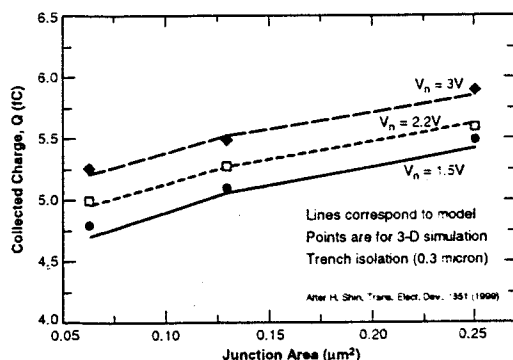
- Charge collection
- Critical charge
- Device area
- 3-D charge collection

Logic Transients Expected for Extreme Scaling

- Noise margin decreases as logic levels drop
- Threshold voltage doesn't scale
 - Clock design is extremely complex
 - Corrects for skew; allows operation at extremely high speed
- Clock, logic design partially overcomes these limitations
 - Corrects for skew; allows operation at extremely high speed
- Logic transients will likely increase processor upset rates to unacceptable levels

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DRAM 3-D Charge Modeling



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Recommendations

Continue to Use Hardened Processors for Spacecraft Control and Critical Data

- RAD6000 is Proven Commodity
 - Reliable level of hardness in space - proven history
 - Does not require periodic testing and qualification
 - Free from strange error modes and crashes

Commercial Processors Attractive for Less Critical Use

- Higher speed, more processing power
- May be turned off or ignored during solar flares
- More work needed to evaluate operational integrity in applications
- Scaling effects may cause error rates to be worse for future generations
- Commercial operating systems introduce complications and higher error rates

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		54	U	27512		0	0	[
) A1-01 n_____ F_____						_____	_____	
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) A1-01 n_____ F_____						_____	_____	
29		78	C	CKR05	33pF 200V 10%	0	2	[
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1 Jet Propulsion Laboratory

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Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 3: Test Approach

Gary Swift

Outline

Philosophical Choices

- Register v. application testing
- "Golden chip" v. self-test
- Buy v. Build test platform

Overview of Approach Taken

- Static memory testing
- Pseudo-static processor testing

Other Considerations

- Use of JTAG boundary scan
- Validation of approach

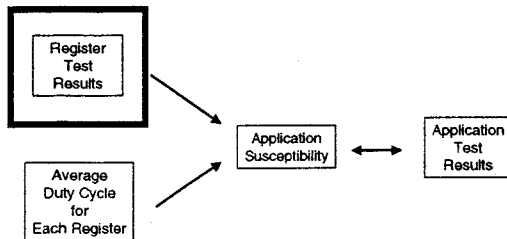
Generic Approach Alternative

- How it works
- Advantages and disadvantages

2

Register v. Application Tests

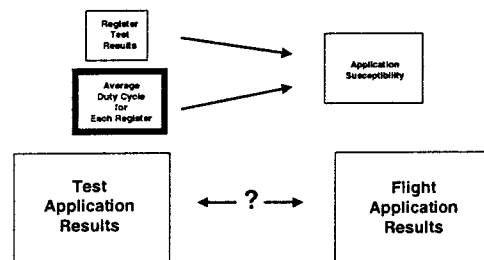
Register Testing Yields "Fundamental" Information



3

Register v. Application Tests

Calculation Of Space Upset Rates



4

Golden chip v. self tests

Finessed this by doing (almost) nothing during the beam

- One word infinite loop during beam- *HERE: Jump to HERE*
- User breaks out with "external interrupt"
- Self-inspection, if any, goes on out-of-beam
- Requires processor functionality post-beam
 - Reset or even power cycle may be okay
- Added half second snapshot stripchart in memory
 - Now "only" 99.9% in infinite loop

Does not preclude virtual golden chip testing later, as needed

5

Buy v. Build Considerations

Evaluation Board allows:

- Test at speed
- Quick to first test
- Adequate to build on (?)

Minimize efforts for Maximum Results

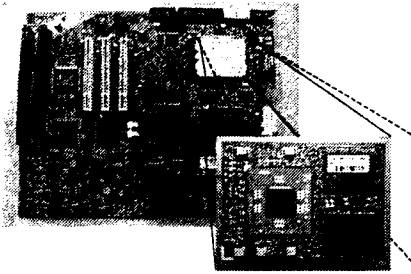
- Minimize custom hardware
- Minimize machine coding

Automate (and Maximize) Data Collection

Leverage Existing Rad Group Resources

6

"Yellowknife" Development Board with Processor/Cache Module (PCM)



7

Buy v. Build Considerations

Evaluation Board allows:

- Test at speed
- Quick to first test
- Adequate to build on (?)

Minimize efforts for Maximum Results

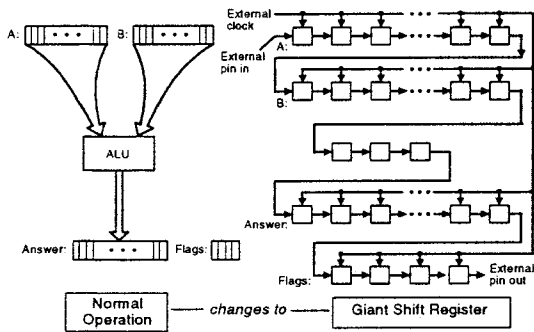
- Minimize custom hardware
- Minimize machine coding

Automate (and Maximize) Data Collection

Leverage Existing Rad Group Resources

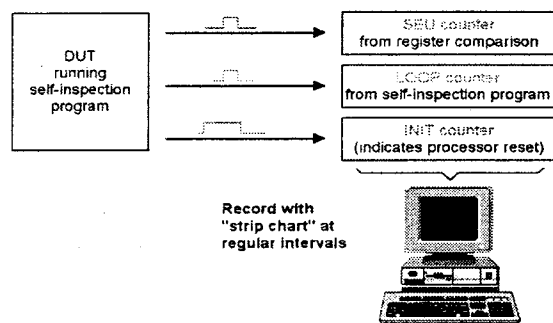
8

Boundary Scan



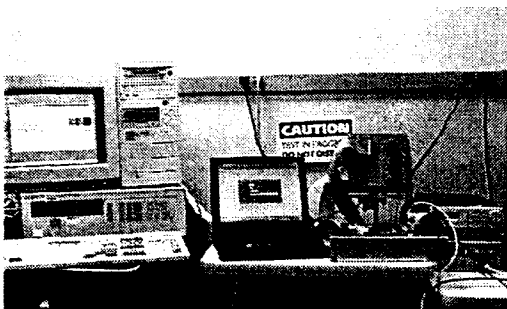
9

Overview of "Pin Wiggler" Method



10

Generic Test Approach: Pin Wiggler



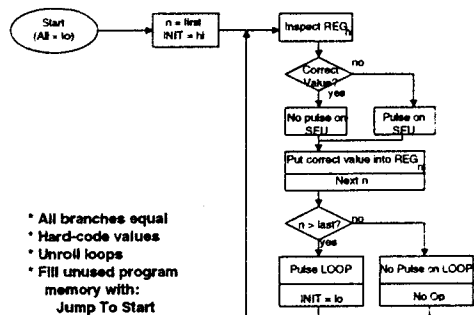
11

Generic Test Approach: Pin Wiggler



12

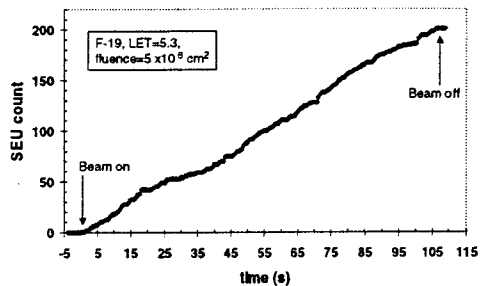
"Pin Wiggler" Self-Inspection Program



- All branches equal
- Hard-code values
- Unroll loops
- Fill unused program memory with:
Jump To Start

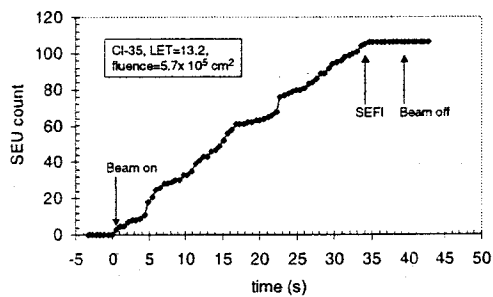
13

Pin Wiggler Example: PIC 16C505 upsets



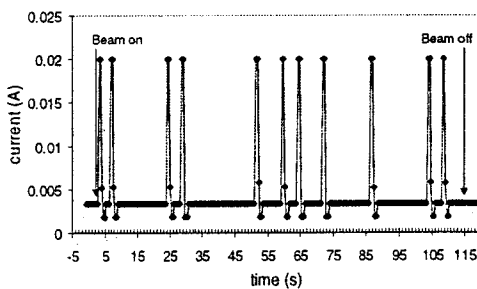
14

Pin Wiggler Example: PIC 16C505 (w/ SEFI)



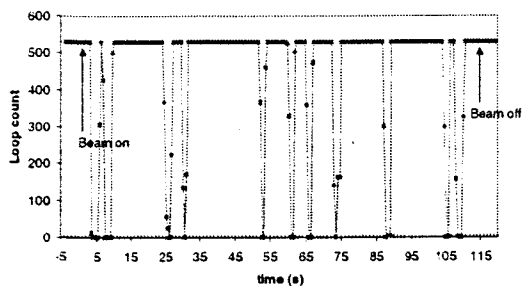
15

Pin Wiggler Example: AIC51 - 11 latchups



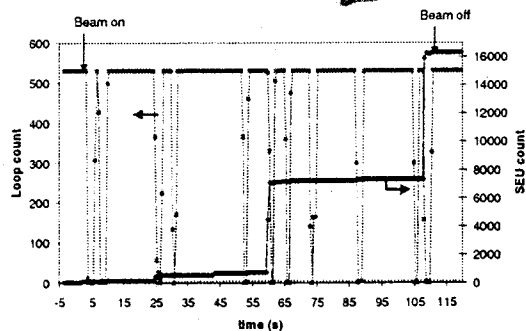
16

Pin Wiggler Example: AIC51 - Loop counter



17

Pin Wiggler Example: AIC51 - Upset results



18

Conclusion

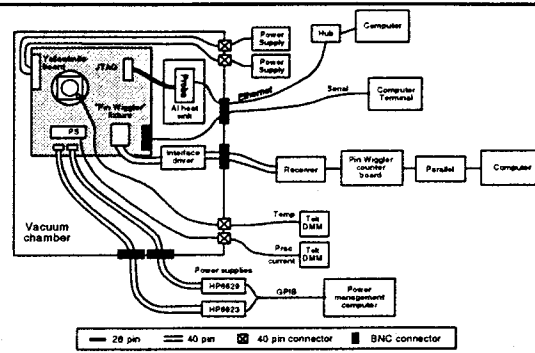
"Pin Wiggler" is:

- simple
- data rich

but has limitations of all register testing

19

Test Approach Using "Yellowknife" Development Board



20

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 4: Proton Test Results

Doug Millward

Outline

Introduction to Proton Testing

Test Facilities

- Indiana University Cyclotron Facility (IUCF)
- UC Davis Crocker Nuclear Laboratory (CNL)

Power PC 750 Proton SEU Data

- Registers (FPR, GPR, SPR)
- L1 Cache
- L1 Cache Tags/Flags

Discrepancy between facilities at 60-65 MeV

Comparison to earlier PowerPC 603e data

2

Introduction to Proton Tests on MPC750

- Proton tests more straightforward than heavy-ion tests.
 - Done in air rather than vacuum
 - Allow easy development and checkout of test hardware/software
 - Provide estimate of device behavior in subsequent HI tests
- Checkout of hardware/software in proton environment indicated significant effect of program "hangs".
 - In our tests, processor needs to run successfully to identify internal errors, therefore program "hangs" limit/negate data
 - Program modified to reduce effect of "hangs"
 - Software modified to minimize processor activity
 - Hardware and software simplified as much as possible
 - Test approach modified to mitigate effect of "hangs"
 - JTAG probe used to capture pre- and post-beam register contents
 - Strip Chart generated showing near real time register contents
 - Use of low-fluence runs produced good data with minimum "hangs"

3

Proton Facilities

Indiana University

- "Raw beam" is 200 MeV
- Lower energies obtained by interposing Cu degraders
- Results in spread of energies, particularly with thick degraders
 - Up to 3.3 cm of copper used to degrade beam
 - Tests with 60-MeV degraded beam overlap maximum energy at Davis

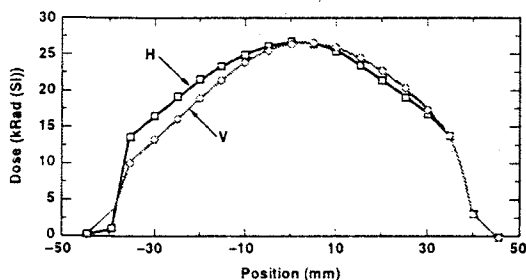
UC Davis

- Beam is tuned to obtain nominal desired energy
- Tuned energies from 15 to 65 MeV
- Corrections for air, window losses, DUT thickness required at lowest energies

4

IUCF Beam Profile

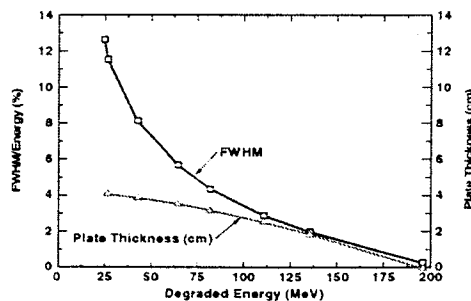
196 MeV Protons



5

Degrader Properties at IUCF

Plate Thickness and % Energy Spread vs Degraded Energy



6

Proton Test Results for MPC750

Registers Tested with Ones or Zeros Loaded

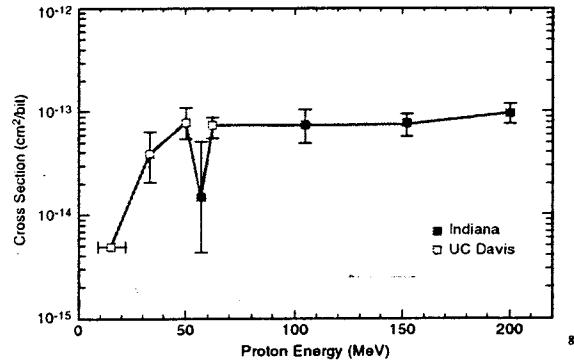
- Saturated cross section 10^{-13} cm²/bit for "1" to "0" transition
 - Cross section approximately three times lower for "0" to "1" transition
 - Explanation not known but probably due to differences in design of register cells and geometry of internal transistors
- Threshold between 30 and 50 MeV

D-Cache Tested with Ones or Zeros Loaded

- Saturated cross section about a factor of two lower than Registers
- Threshold below lowest energy used at UC Davis (~20 MeV)
- No significant differences observed between Ones or Zeros
- L1 Cache Tags/Flags behave in a similar manner to Cache
- Explanation based on use of small-area devices
 - Smaller saturated cross sections
 - Smaller Q_{crit} implies lower recoil energy deposition (from nuclear interaction) needed to produce upset

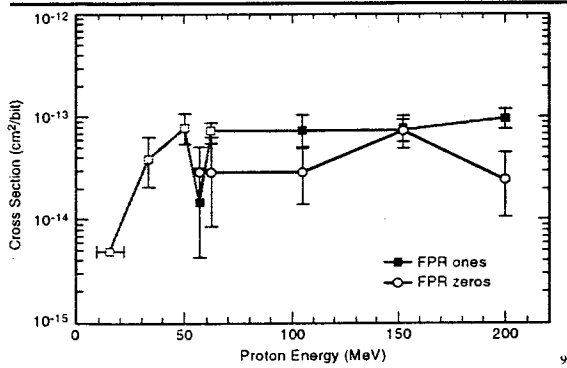
7

Upset Cross Section for FP Registers ("1" transitions)



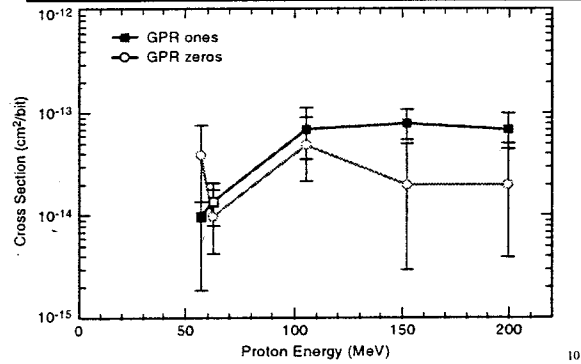
8

Upset Cross Section for FP Registers (both transitions)



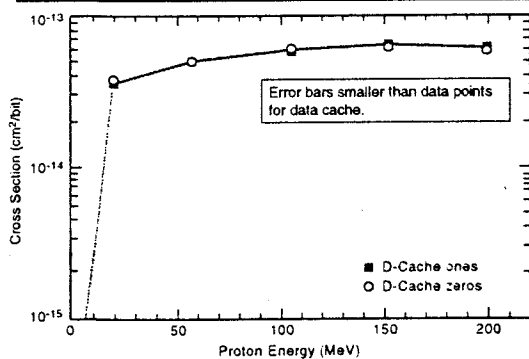
9

Upset Rates for General-Purpose Registers



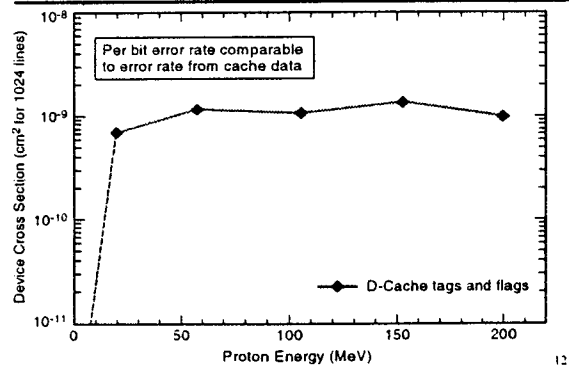
10

Proton Cross Section for Data Cache



11

Proton Cross Section for D-Cache Tags and Flags



12

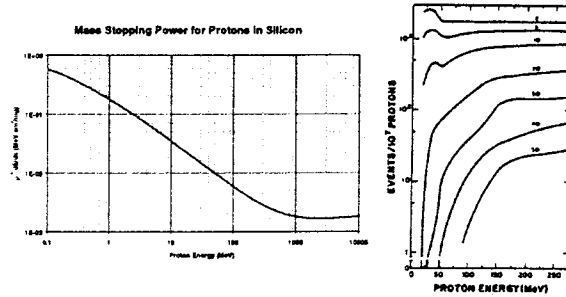
Discrepancy Observed at 60-65 MeV

Differences seen in SEU cross sections between IUCF and UC Davis at 60-65 MeV

- σ_{IUCF} approximately five times less than σ_{UCD} at 60-65 MeV
- Possible explanations include:
 - Low-energy contamination of IUCF beam
 - Energy spectroscopy would determine amount of low-energy protons present
 - Poisson statistics
 - Error in Cu degrader thickness
 - Measurement errors

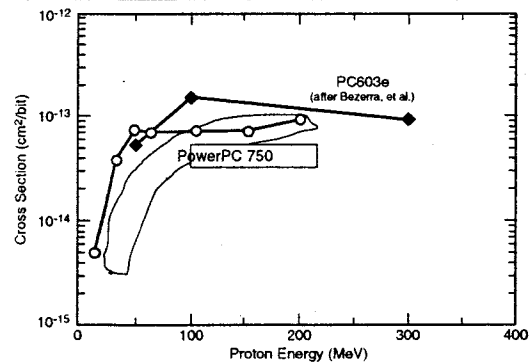
13

Energy Dependence of Proton dE/dx (Dose) and Proton SEU Error Rate (Nuclear Reaction σ)



14

Comparison of Proton SEU Cross Sections for PowerPC750 and PC603e



15

Summary and Conclusions

Initial experiments performed at proton facilities allowed checkout of test approach and modification of hardware and software in simple particle environment.

Discrepancy has been noted between SEU cross section measured at IUCF and UC Davis.

Upset susceptibility of MPC750 registers is 3x higher when storing 1's relative to storing 0's. Energy threshold is ~15 MeV.

Upset susceptibility of L1 data cache bits is symmetric, and the energy threshold is below 15 MeV.

Upset of L1 cache Tags/Flags remarkably similar to L1 cache data bits.

16

Dealing with "Hangs"

"Hangs" Interfere with Error Rate Measurements

- Affect statistical uncertainty of measurements
- Difficult to categorize

Ways to Minimize Effect of "Hangs"

- Use very simple test algorithms
- Validate partial runs

13

Dealing with Thermal Problems



14

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 7: Heavy Ion Results

Steve Guertin

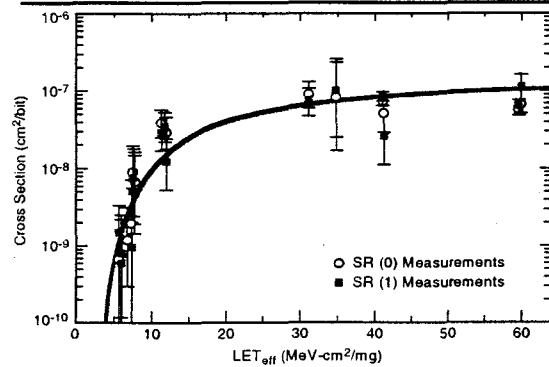
Outline

- Specific Register Results
- Cache Results
- Processor Comparison
- Concluding Remarks

2

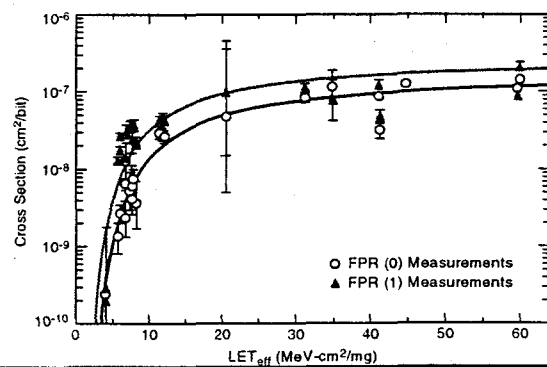
SEU Cross Section for Special Purpose Registers

(note: Low LET results mostly "pin wiggler" data)



3

SEU Cross Section for Floating-Point Registers



4

Practical Testing Issues

Flip-Chip Bonding

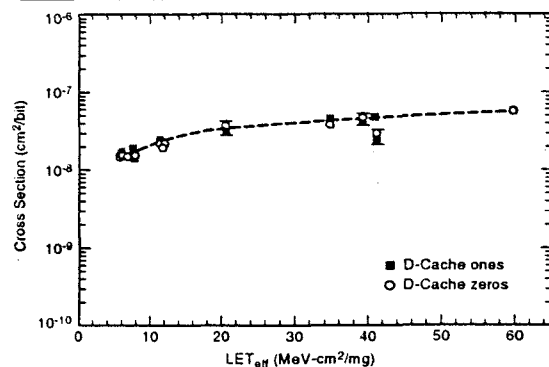
- Eliminates ability to "delid" device
- SEU testing still possible with extremely energetic ions
- Back irradiation provides an alternative approach
 - Mechanical "thinning" reduces range requirement
 - May not be equivalent to top irradiation

Power Dissipation

- Power PC750 dissipates 6W at full speed
- Difficult issue in vacuum chamber
- Heating may be worse for thinned samples

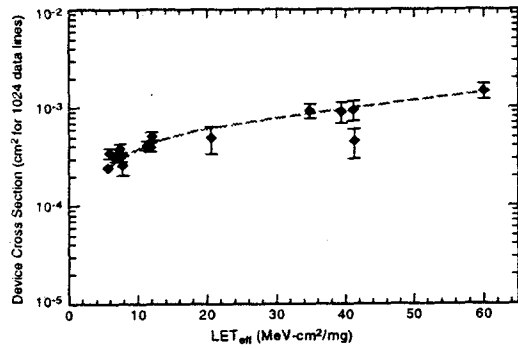
5

Upset Cross Section for Data Cache



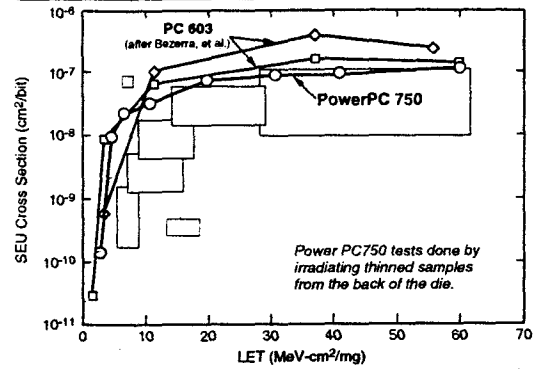
6

Upset Cross Section for Cache Tags and Flags



7

Comparison of SEE Cross Sections for the PowerPC 750 and PC603e



8

Conclusions

- Registers storing 1's are more susceptible than those storing 0's. This is consistent with the proton results.
- Cache bits are equally susceptible whether storing 1's or 0's. This is also consistent with the proton results.
- The L1 data cache tags and flag are roughly the same susceptibility as the cache bits themselves. At this time, the testing does not separate the susceptibility of 1's and 0's.

9

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 8: Proton/Heavy Ion Results Comparison

Larry Edmonds

Outline

- Introduction
- Model for Obtaining Proton Results from Heavy Ion Data
- Model Results vs. Published Data
- PowerPC Results of the Model
- Conclusions

2

New Work Compared to Previous Work on the Proton/ Heavy Ion Relationship

All results previously derived from physical analysis (as opposed to empirical fits):

- Assume the RPP model
- Require supplemental information (RPP thickness or critical charge) in addition to heavy ion data for predicting proton cross sections.

New Work:

- Uses a more realistic physical model (a continuous charge-collection efficiency function instead of RPPs)
- Gives upper bound proton cross section estimates derived from heavy ion data (no supplemental information or fitting parameters required.)

3

A Relationship from Charge Collection Physics

Equation:

$$\sigma_{pr}(E) \leq \frac{\beta(E)}{a} \int_0^{\infty} \frac{1}{L} \frac{d\sigma_{hi}(L)}{dL} dL$$

where a is a constant and $\beta(E)$ is from a table

From:
L.D. Edmonds, "Proton SEU Cross Sections Derived from Heavy-Ion Test Data,"
IEEE Trans. Nucl. Sci., vol. 47, no. 5, pp. 1713-1728, Oct. 2000.

4

Comparison with Published SEU Results

PART	DATA $\sigma_{SEU} (cm^2)$	MODEL $\sigma_{SEU} (cm^2)$	RATIO
SMJ44100	7.0E-7	1.9E-8	2.7
9226R	1.5E-7	3.8E-7	2.8
IBM 16MEG	2.1E-8	5.8E-8	2.7
MT4C1004C	3.9E-7	1.0E-6	2.5
KV41C4000Z-8	3.3E-7	8.9E-7	2.7
O1G9274	4.2E-9	3.1E-8	7.4
OW 92258	3.7E-8	2.3E-7	2.8
MT4C4001	2.9E-7	1.2E-6	4.1
HM6116	4.8E-8	4.7E-8	1.0
92932H	2.9E-8	5.0E-8	1.7
29018	8.5E-10	2.1E-9	2.5
TCS14100Z-10	1.0E-8	2.0E-8	2.0
HM 95658	3.0E-8	9.8E-8	3.2
VB814100 10PSZ	8.9E-7	2.9E-6	4.2
HY8514100J	1.5E-6	2.5E-6	1.7
LuN C	2.1E-8	8.2E-8	3.9
D424100V-80	1.8E-8	2.3E-8	1.3
HM6518	2.5E-9	1.6E-8	6.5

5

Comparison with Published Results (cont'd)

SEU (per bit):

PART	DATA $\sigma_{SEU} (cm^2)$	MODEL $\sigma_{SEU} (cm^2)$	RATIO
Farchid 33L422 Bipolar	1.4E-10	9.6E-11	0.70
Samsung 16Mb 3.3V DRAM	3.5E-14	7.4E-14	2.1
Hitachi 16Mb 3.3V DRAM	1.6E-14	2.4E-14	1.5
Vicron 16Mb 3.3V DRAM	8.0E-15	1.9E-14	2.3
BM 16Mb 3.3V DRAM	1.7E-15	2.8E-15	1.6

Latchup:

PART	DATA $\sigma_{SEU} (cm^2)$	MODEL $\sigma_{SEU} (cm^2)$	RATIO
AMD K5 microprocessor	5.6E-9	1.9E-8	3.4
HM65162 (1985)	1.4E-10	2.9E-8	210

6

Checking PowerPC 750 Results

Registers were tested with both protons and heavy ions.

- Proton data at energies up to 51 MeV show the shape of the curve well enough to extrapolate. Extrapolating gives a saturation cross section of $\sim 1 \times 10^{-13} \text{ cm}^2/\text{bit}$.
- Heavy ion data used with the model predicts a proton saturation cross section of $1.3 \times 10^{-13} \text{ cm}^2/\text{bit}$ for the registers.

7

Conclusions

The upper bound estimate for the proton cross section is very nearly equal to the actual cross section measured for the PowerPC 750 registers.

8

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 9: Space Environments

Allan Johnston

Outline

• Introduction

• Model Environments for REE

- How Rates Are Calculated
- Rate Results
- Conclusions

2

Coming Attractions

REE Fault Model Overview	Arbi Karapetian
Error Rate Calculation	Larry Edmonds
Error Rate Results	Gary Swift
Conclusion and Near-Term Plans	Gary Swift
Discussion	Reviewers

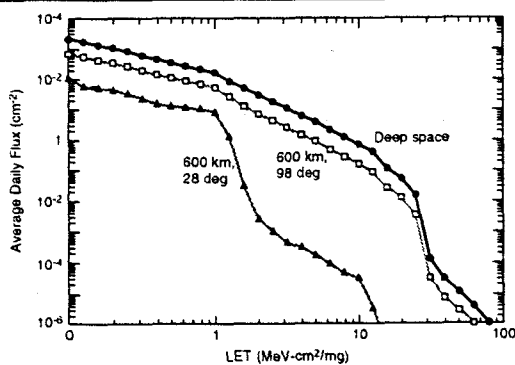
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Specific Missions Considered for REE Applications

- Deep Space
- Surface of Mars
- 600 km, 98° Polar Orbit
- 600 km, 28° Polar Orbit

4

Galactic Cosmic Ray Spectra for Different Environments



5

Solar Flares

JPL Uses a Specific Flare for Design Purposes

- GCR fluence approximately 1/ 10 that of October 1989 flare
- Exponential time model ($\tau = 20$ hours)

Proton Fluence

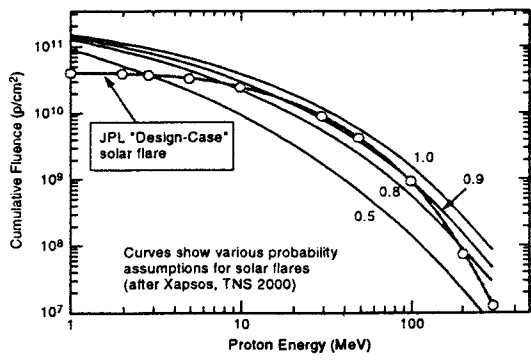
- Total fluence = $\times 10^{10}$ p/cm² (> 30 MeV)
- Corresponds to $P = 0.1$ on Xapsos probability model

Error Rates Calculated on Basis of 24-Hour Day

- Peak error rates during the first few hours of a flare are higher
- Conventional SEE rates usually reported in errors/bit-day

6

Proton Spectrum Compared with Xapsos Model



**Radiation Evaluation of the PowerPC 750
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Section 10: Overview of the Fault Model

Arbi Karapetian

Outline

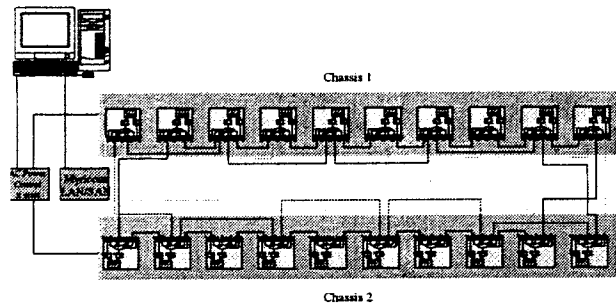
Overview of the Fault Model

Inputs and Outputs

Fault Model Results

The REE System

JPL

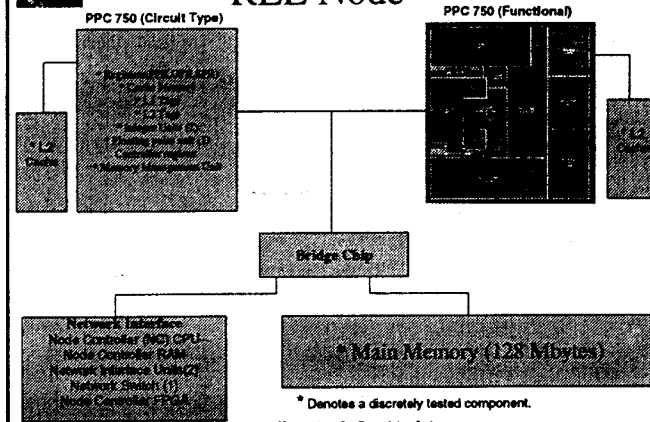


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REE Node

JPL



APRIL 25, 2001

Karapetian, Jet Propulsion Laboratory

REE Fault Model

JPL

- Inputs:** Per bit fault rates; Specific to space environment, and specified subsystem (i.e. PCI bridge chip, caches, microprocessor subsystems, memory, etc.)
- Outputs:** Fault rates in specific environment, for REE system, REE node, microprocessor, and lower level subsystems as necessary.

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Assumptions and considerations

JPL

- The Following discrete items have been tested on the Motorola PPC750 Microprocessor:
 - Memory Management Unit (MMU) Translation Look-aside Buffers (TLBs)
 - Registers: FPR, GPR, and SPRs
 - L1 Cache Data bits
 - L2 Cache Data bits
 - L1 Cache Tags & Flags
 - L2 Cache Tags & Flags
- Analysis of available data on the above regions, shows two circuit types in the PPC750 with distinct SEU rates. Register types, and Cache(memory) types.
- The Bridge Chip and the Network Interface chips have not been tested, and are scheduled to be tested in the current fiscal year. An estimation of circuit types in these chips has been made, and numbers from similar circuit types in the PPC750 have been used to calculate fault rates for these chips in the fault model.
- There are a number of unexplained "hangs" while irradiating the PPC750 microprocessor during experiments, which are currently under investigation by the JPL Radiation Testing Group.
- Gate Fault Rates have not been observed in the laboratory experiments. The fault model currently uses a factor of 0.00001 latch fault rates, as a place holder. In the event laboratory experiments show a different number, or verify a zero fault rate, this number can be changed to update the fault rates.

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Latch and Gate calculations

JPL

Two methods of calculating Latch and Gate counts

First Method (Higher Accuracy):

- From Power PC750 Manuals, extract the number of registers in each functional device (i.e. GP registers, FP registers etc.), extract corresponding widths (in bits), and get total number of bits.

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Second Method (Lower Accuracy):

JPL

- We know there are 6.35×10^6 transistors in the Power PC 750. At 4 transistors/Gate = 1.6×10^6 Gates
- We can estimate the percent area of each chip subsystem, by measuring the corresponding die overlay region. (i.e. Integer Units, Floating Point Unit, etc.)
- Multiply the percent area from total, of the corresponding chip subsystem by total gate count (1.6×10^6) to get the number of gates for the chip subsystem.
- Use an average gate to latch ration of 30 gates for each latch, to calculate the number of latches in that region. (1st order approximation, to be revised in the future)

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Why have the fault Model?

- The fault model results will be verified against radiation experiments in laboratory radiation experiments of the system, and flight experiments, in order to validate the results.
- To estimate fault rates, for devices which are not accessible directly, or have not yet been tested.
- To extrapolate fault rates, for next generation processors.

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Sample calculation sheet for Latch Faults (First Method)

CPU area mode		1587500	9.54E-12	
Gate count				
Gate fault rate (GFR)				
Totals:		33760.8	100	1587500
instruction sequencer		6360.83	15.8	1587500
integer units		4127.5	7.8	1587500
floating point unit		5503.33	10.4	1587500
load/store unit		4296.25	8.1	1587500
L1 D-cache		different density	10.6	1587500
L1 I-cache		different density	13.1	1587500
Dtags		different density	2	1587500
Itags		different density	2	1587500
L1 D-cache control		1217.08	2.3	1587500
L1 I-cache control		793.75	1.5	1587500
MMU TLBs		different density	1.3	1587500
IMMU TLBs		different density	1.3	1587500
L2 cache tags		different density	5.9	1587500
L2 cache control and bus VI		3280.83	6.2	1587500
PLL		476.25	0.9	1587500
TAU		264.583	0.5	1587500
unknown		5450.42	10.3	1587500

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Fault Model Results

Average Rates (Fault/Hour)

	Mars Surface	Earth Orbit (600Km-28°)	Interplanetary Space (Solar Minimum)	Interplanetary Space (Solar Maximum)	Interplanetary Space (Solar Min. w/Flare)
Single REE Node (100 Mil Al Shielding)	0.02	0.21	0.25	0.07	192.4
20 Node REE System (100 Mil Al shielding)	.34	4.14	4.97	1.33	3852.98

$$\text{Environmental SEU rates per bit From Radiation Tests (specific to circuit type)} \times \text{Number of bits in each functional block (Specific to circuit type)} = \text{Total Fault Rate in Specified Environment Per functional block}$$

$$\text{REE Node Fault Rate in Specified Environment} = \sum_{\text{All Functional Blocks in REE Node}} \text{Total Fault Rate in Specified Environment Per functional block}$$

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Radiation Evaluation of the PowerPC 750 Microprocessor

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Section 11: Error Rate Calculations

Larry Edmonds

Outline

- Introduction
- Model Environments for REE
- **How Rates Are Calculated**
- Rate Results
- Conclusions

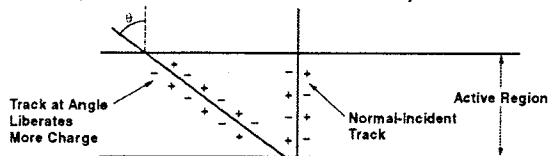
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SEU Rate Depends on How Cross Section Varies with Both Ion LET and Incident Angle

Cosine law is usually assumed when plotting test data.

- Applies when active regions are thin enough so that lateral variations in the charge-collection efficiency can be ignored when comparing two points on the same track.

- The relevant quantity is liberated charge per perpendicular depth, so the effective LET is ion LET divided by $\cos\theta$.



3

SEU Rate Depends on How Cross Section Varies with Both Ion LET and Incident Angle (cont.)

- Often an adequate approximation for suitably restricted tilt angles.

But the active region is not always thin enough for lateral variations in the charge-collection efficiency to be unimportant, so the cosine law has limitations.

- Should always fail at some sufficiently large tilt angle.
- Sometimes fails even at small angles.

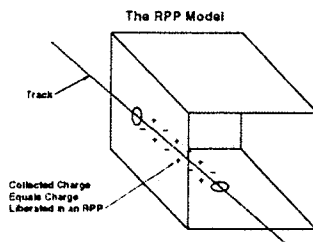
Therefore, a more versatile model is needed for SEU rates.

4

The RPP Model

The traditional model is the RPP model. It assumes that:

- Charge collected at a device node is the charge liberated within an associated RPP.



5

The RPP Model (cont.)

- A device contains a collection of geometrically identical RPPs but with different susceptibilities, i.e., different critical charges that collected charge must exceed for an upset.

- The gradual increase in a device cross section curve with increasing LET is from an increasing number of contributing RPPs.

6

Physics Doesn't Matter Because the RPP Model is Just a Fit

The assumptions behind the RPP model are not physically correct.

- Charge collected from ionization at a given location varies continuously as the location is varied.
- The increase in device cross section with increasing LET is largely, if not almost entirely, from an increase in each bit cross section, as opposed to an increase in the number of contributing bits.
- In particular, the physical assumptions behind the RPP model do not predict multiple bit upsets from charge sharing.

The assumptions don't have to be correct because use of the model is analogous to curve fitting.

7

Physics Doesn't Matter Because the RPP Model is Just a Fit (cont.)

The only requirement is that the dependence of cross section on LET and direction be correctly described.

The goal is to select model parameters that will produce a fit to measured data.

- A perfect fit to the normal-incident cross section versus LET curve can be obtained by selecting an appropriate distribution of critical charges.
- The directional dependence of the cross section is another issue.

8

Directional Dependence Implied by the RPP Model

The parameter describing the directional dependence is the ratio R of lateral dimensions to thickness (the two lateral dimensions are usually assumed to be equal).

- Very large R gives the cosine law.
- $R=1$ approximates an isotropic cross section.
- $R=5$ approximates the cosine law up to about 60° , with progressively larger deviations from the cosine law at larger angles.

The objective is to select the R that best describes the directional dependence (either measured or assumed) for the device considered.

9

A Source of Error

The RPP thickness need not be the dimension of any physical structure.

Therefore, the appropriate R should be determined from knowledge of the directional dependence of device cross section.

Unfortunately, test-ion range limitations prohibits testing at large angles, so there is almost always some uncertainty in the directional dependence.

10

A Source of Error (cont.)

Unfortunately, predicted SEU rates for hard devices are very sensitive to the assumed directional dependence.

- For example, one assumption regarding the directional dependence may predict that a hard device is completely immune to iron, while another assumption predicts upsets from hits by iron at sufficiently large angles.
- The two assumptions predict very different SEU rates.

Fortunately, predicted SEU rates for soft devices are less sensitive to the assumed directional dependence (e.g., all assumptions agree that hits by iron, at any angle, will upset very soft parts).

11

For The PowerPC 750 Case...

• All PC750 tests were at normal or near-normal incidence, so there is no indication of the directional dependence. But the device is soft enough so that predicted SEU rates are fairly insensitive to R .

• In the absence of conflicting information, we sometimes use $R=5$ as a best guess.

• A worst-case R is a trial-and-error selection to obtain the largest calculated rate (almost always produces the cosine law).

• Rates calculated from the two above R 's differ by about a factor of two (or less, depending on the environment) for the PC750.

• Close enough to not warrant additional investigation. The $R=5$ rates were chosen.

• However, additional tests at angles might show that the estimates are too conservative (e.g., if the cross section is nearly isotropic). This might be a motivation for additional tests.

12

A Caveat...

The D Cache data do not extend to low enough LET to show the shape of the cross section curve. Some modeling was used.

The cross section curve was described by a two-parameter curve (from diffusion theory) [1] instead of the four-parameter Weibull function because:

- The former curve was derived from charge transport physics while the Weibull function was not.

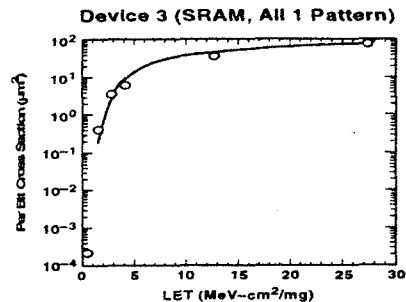
- If the device cross section is the sum of cell cross sections i.e., tests count upsets instead of upset clusters when there are multiple-bit upsets.

And: Data are free of cosine-law errors.

Then: Data do not saturate as fast as the Weibull function, and fit the two-parameter curve better.

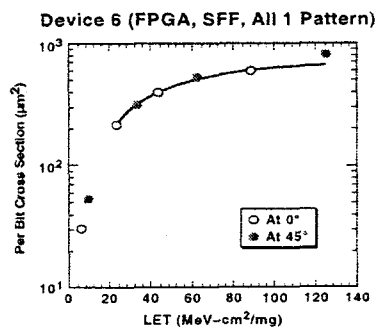
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New Model Fit Example



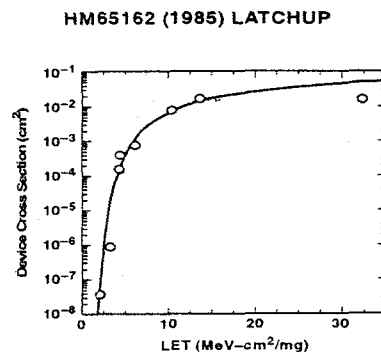
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New Model Fit Example



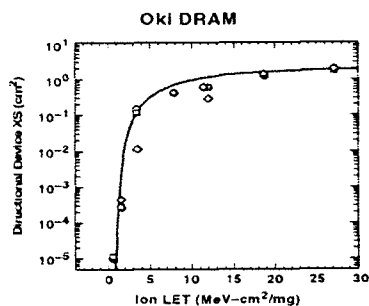
15

New Model Fit Example



16

New Model Fit Example



17

A Caveat... (cont.)

The two parameters were selected to:

- Fit the available heavy-ion data.
- Make the proton cross section derived from heavy-ion data [2] agree with the measured proton cross section.

Real data would be better.

- Predicted rate is sensitive to the way the data are extrapolated to lower LET.
- Calculated rate could be too small.
- Additional testing is needed.

[1] L.D. Edmonds, "SEU Cross Sections Derived from a Diffusion Analysis," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 4, pp. 3207-3217, Dec. 1996.
 [2] L.D. Edmonds, "Proton SEU Cross Sections Derived from Heavy-Ion Test Data," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 5, pp. 1713-1728, Oct. 2000.

18

Proton Rates

Cross section for protons is assumed to be isotropic, so proton rates are calculated by simply integrating the cross section (a function of proton energy) with the proton spectrum.

Rates from trapped protons dominate rates from heavy ions at low latitudes.

- Geomagnetic shielding attenuates the heavy ion spectrum.
- Severe proton environment during passes through the South Atlantic Anomaly (SAA).

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 11a: Error Rate Calculations - Appendix

Charge Collection Fundamentals:
The Importance of Diffusion

Larry Edmonds

The First Step After an Ion Hits a DR

After an ion hits a reversed-biased pn junction depletion region (DR), the first step is a DR collapse.

- Some of the liberated carriers are rearranged by the strong electric field in the DR until the formerly unshielded impurity (doping) ions become shielded.
- What was formerly a space charge region (the pre-hit DR) is now quasi-neutral, i.e., the DR is essentially removed.
- Only a small fraction of the liberated carriers are needed to do this. Nearly all of the initial track is intact and in a quasi-neutral region.

2

The First Step After an Ion Hits a DR (cont.)

The collapse stage is effectively instantaneous from the point of view of charge collection at the device contacts.

- The rearrangement of carriers in the device interior is so fast that it is accompanied by very little charge collection at the device contacts.
- The significance of the collapse stage is to set up the initial conditions for the recovery stage that follows

3

The Recovery Stage

Nearly all charge collection at the device contacts is during the recovery stage.

At the start of the recovery stage, the DR width is almost zero, so essentially all of the track is outside the DR (in the quasi-neutral region).

Carriers in the region formally occupied by the pre-hit DR are not "promptly" collected because they are outside the post-hit DR.

As recovery progresses, the DR boundary (DRB) gradually moves deeper into the device interior as the DR gradually regains its original width.

4

A Low-Order Approximation for Charge Collection

A particular approximation for charge collection has been called "low-order" because it ignores DRB motion.

The strong electric field in the DR prevents majority carriers from entering it.

- Under static conditions (no DRB motion), this implies that there is zero majority-carrier current in the quasi-neutral region near the DRB.
- Therefore, the potential distribution in the quasi-neutral region becomes whatever it must be to make the majority-carrier drift current balance the majority-carrier diffusion current (the existence of a potential distribution in the quasi-neutral region has been called "funneling").

5

A Low-Order Approximation for Charge Collection (cont.)

Ion hits produce high-density conditions (the carrier density greatly exceeds the doping density).

- Under high-density conditions, the electron and hole densities have nearly equal values and gradients in the quasi-neutral region.
- Therefore, majority-carrier drift being equal to majority-carrier diffusion near the DRB implies that minority-carrier drift equals minority-carrier diffusion near the DRB.
- But the minority-carrier currents add to instead of subtract from each other, so half of the total current is minority-carrier drift, and the other half is minority-carrier diffusion.
- Stated another way, the current is twice the minority-carrier diffusion current.

6

A Low-Order Approximation for Charge Collection (cont.)

To the extent that the low-order approximation applies, the current is twice the minority-carrier diffusion current [1],[2].

DRB motion upsets this condition and is one source of error in the low-order approximation.

- [1] L.D. Edmonds, "Charge Collection from Ion Tracks in Simple EPI Diodes," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 3, pp. 1448-1463, June 1997.
 [2] L.D. Edmonds, "Electric Currents Through Ion Tracks in Silicon Devices," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 3153-3164, Dec. 1998.

7

Calculating the Diffusion Current

The diffusion current is calculated from the minority-carrier diffusion coefficient together with the gradient of the carrier density.

The gradient is calculated by solving an equation together with boundary conditions.

The equation describing the carrier density (not flow, but density) is the ambipolar diffusion equation.

8

Calculating the Diffusion Current (cont.)

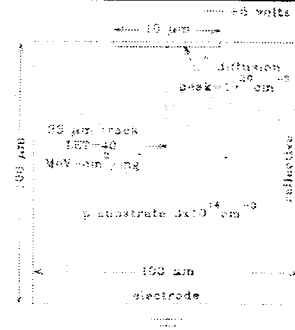
Boundary conditions are from another approximation.

- Although high-density conditions apply at the DRB, the carrier density there is still much less than elsewhere on the track.
- Therefore, an approximation treats the DRB as a sink, i.e., the carrier density there is approximated as zero for the purpose of estimating the gradient from the diffusion equation.
- This is another source of error in the low-order approximation.

9

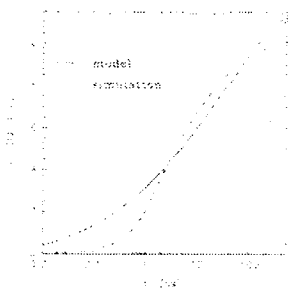
Comparison with a Simulation Result

A simple diode was simulated: a device with rotational symmetry.



10

Comparison with a Simulation Result (cont.)



Comparison of collected charge calculated from the low-order approximation to the simulation prediction.

11

Comparison with a Simulation Result (cont.)

For t less than 2 ns, the low-order approximation predicts too much current.

- The assumed sink-like boundary condition is a bad approximation at very early times.
- The over-estimation in the current persists for less than two-tenths of a nanosecond, but the collected charge is cumulative, so its error persists for a longer time.

12

Comparison with a Simulation Result (cont.)

Then the curves come together.

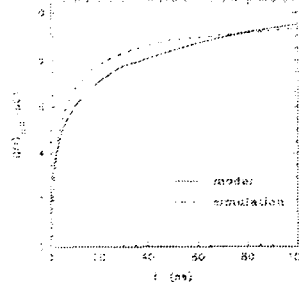
- DRB motion enhances the actual current, but is not included in the model, so the actual collected charge catches up to the model prediction at about 2 ns.
- The curves then stay fairly close together until 100 ns.

The curves diverge again after 100 ns.

- The model assumes high-density conditions for all t , which is incorrect at very large t .
- Most of the charge that ever will be collected was collected during the first one-hundred ns, so the erroneous assumption produced only a moderate error in the predicted collected charge.

13

Comparison with a Simulation Result (cont.)



If the time scale of interest is measured in nanoseconds up to 100 ns, the agreement can be made to look better by using a linear time axis

14

Comparison with a Simulation Result (cont.)

- If Fig. 3 adequately represents the time scale of interest, then the low-order approximation, which is a diffusion calculation, did a pretty good job.
- For other time scales that might be of interest, the diffusion calculation predicted too much current.
- While erroneous assumptions can make the calculated collected charge from diffusion too large, it is never negligible compared to the actual collected charge.
- Diffusion is always important.

15

Radiation Evaluation of the PowerPC 750 Microprocessor

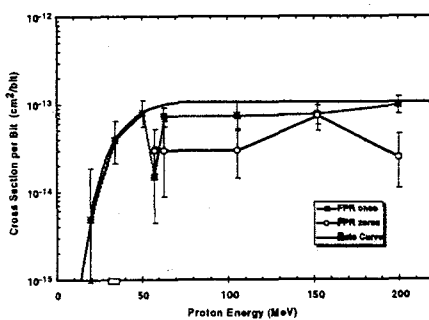
External Peer Review
Section 12: Error Rate Results
Gary Swift

Outline

- Introductory Remarks
- Model Environments for REE
- How Rates Are Calculated
- **Rate Results**
- Conclusions

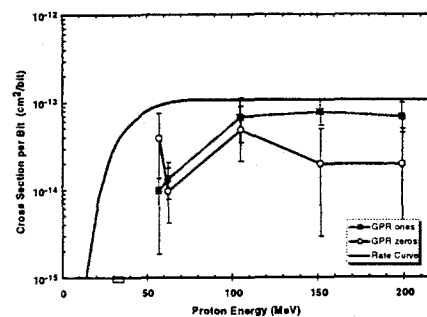
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Proton Model Fit



3

Proton Model Fit (cont.)



4

Approach Used for Rate Calculations

Modified "RPP" Model

- Assumes "cosine law" applies to angles of 70°
- No explicit assumption of collection depth
- Charge at more extreme angles generally "shared" with other nodes

Power PC750 Has Shallow Epitaxial Region

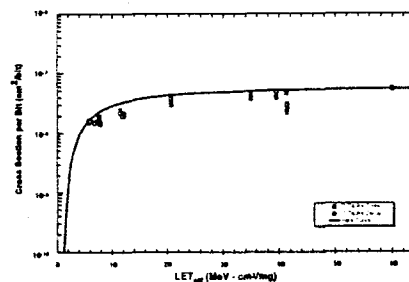
- Reduces charge collection from remote regions
- Also reduces importance of charge diffusion at later times

Other Devices May Have Thicker Charge Collection Regions

- Most advanced commercial memories use bulk substrates
- Complicates charge collection issue and assumptions

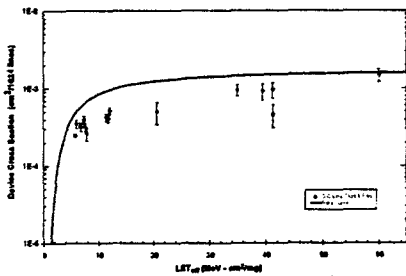
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Heavy Ion Model Fit



6

Heavy Ion Model Fit (cont.)



7

Processor Error Rates for Registers

Space Environment	Errors per bit-day
Interplanetary Space	
Solar minimum GCR	9.4E-7
Solar maximum GCR	2.3E-7
Flare (100 mil shield)	3.5E-4
Martian Surface	5.5E-8

8

Processor Error Rates for Registers

Space Environment	Errors per bit-day
Earth Orbiter (600 km, 28 degree)	
GCR	1.5E-8
Trapped Protons	5.7E-7
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	2.4E-7
Solar maximum GCR	7.2E-8
Trapped Protons	2.7E-7
Flare (100 mil shield)	5.8E-5

9

Processor Error Rates for Registers

Space Environment	Errors per bit-day
Interplanetary Space Flare (protons + ions)	
Shield Thickness (Al equiv.)	
60 mil	2.0E-3
100 mil	3.5E-4
250 mil	1.9E-4
Earth Orbiter (600 km, 98 degree)	
Shield Thickness (Al equiv.)	
60 mil	5.0E-4
100 mil	5.8E-5
250 mil	3.5E-5

10

Peak Rates for Registers

Space Environment	Ratio Peak-to-Average Daily Rate
Interplanetary Space	
Flare (100 mil shield)	4.6
Earth Orbiter (600 km, 28 degree)	
GCR	1.0
Trapped Protons	32
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	3.9
Solar maximum GCR	3.2
Trapped Protons	67
Flare (100 mil shield)	28

11

Processor Error Rates for Data Cache

Space Environment	Errors per bit-day
Interplanetary Space Flare (protons + ions)	
Shield Thickness (Al equiv.)	
60 mil	1.9E-3
100 mil	3.8E-4
250 mil	1.8E-4
Earth Orbiter (600 km, 98 degree)	
Shield Thickness (Al equiv.)	
60 mil	4.8E-4
100 mil	8.0E-5
250 mil	3.5E-5

12

Data Cache Error Rates

Space Environment	Errors per bit-day
Interplanetary Space	
Solar minimum GCR	7.0E-7
Solar maximum GCR	1.9E-7
Flare (100 mil shield)	3.8E-4
Martian Surface	5.0E-8

13

Data Cache Error Rates

Space Environment	Errors per bit-day
Earth Orbiter (600 km, 28 degree)	
GCR	1.7E-8
Trapped Protons	3.7E-7
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	1.9E-7
Solar maximum GCR	6.4E-8
Trapped Protons	1.8E-7
Flare (100 mil shield)	8.0E-5

14

Data Cache Peak Error Rates

Space Environment	Ratio Peak-to-Average Daily Rate
Interplanetary Space	
Flare (100 mil shield)	4.2
Earth Orbiter (600 km, 28 degree)	
GCR	1.0
Trapped Protons	30
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	3.7
Solar maximum GCR	3.0
Trapped Protons	61
Flare (100 mil shield)	20

15

Conclusions Space Error Rates for PC750 at Chip Level

Deep Space (Galactic Cosmic Rays)

- Errors in registers and cache approximately every other day
 - Without cache, errors approximately every month
 - However, turning off cache adversely affects performance
- Crashes may also occur (can't quantify well at this stage)

Solar Flare

- Error rates approximately 400 times higher
- Several hundred errors during "design-case" flare (24 hours)

Earth Orbiting Applications

- Daily average rate higher, dominated by trapped protons
- Solar flare increases error rate by factor of 40

16

Conclusions

• Proton rates tend to dominate heavy ion rates for environments with significant proton components:

- Earth Orbit (due to trapped protons)
- Large Flares

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Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 13: Plans & Conclusions

Gary Swift

Recent Testing

Tests of TLB's (page table cache)

- Low energy proton at UC Davis
- Heavy ion testing at Texas A&M

Tests of G4 (MPC7400)

- Low energy proton at UC Davis
- Heavy ion testing at Texas A&M

Tests of IBM PPC750

- Heavy ion testing at Texas A&M

Tests of L2 Tags & Flag

- Low energy proton at UC Davis
- Heavy ion testing at Texas A&M

2

Next Steps

Complete Motorola XPC750 Tests

- High energy protons of TLB's and L2 tags and flag
- Fill in heavy ion LET "holes" in data, especially very low LET
- More tests of L1 instruction cache
- Develop branch table cache test (?)

Associated Circuitry

- Complete three manufacturers' cache SRAMs
- Begin testing a PCI bridge chip
 - Socketing yellowknife has not worked
 - Must build custom test card

Complete tests of IBM PPC750 and Motorola G4

3

Next Steps (cont.)

More dynamic operations testing (using FPU test)

- Find LET threshold
- Look for scaling effects using G4
- Look for scaling effects using smaller 750

4

Further Steps

Conduct a major campaign investigating hangs

- Developing custom hardware to halt processor immediately
- Capturing device pin states with logic analyzer
 - Any illegal states ??
 - When do errors (and what types) propagate to the pins?
- Can more types of hangs be caught ?
 - More trapping possible ?
 - At least, identify and classify more types

Continue to push toward fully understood "application testing"

- Can error model be validated this way?
- Error detection in "new" programs possible?

Test scaled versions of PowerPC family for comparison

5

Known Problem Areas

Need tests of angular response to heavy ions

- Experimental data is critical to upset rates (validate or invalidate that $R=5$ for RPP aspect ratio)

Need to analyze data for:

- Hang information and ballpark rates
- Multiple upset bits from single events
- Different register responses, especially within SPR type

Need to measure lower LET cross sections

- Upset rate is particularly sensitive to our assumptions here

Could investigate 60 MeV proton discrepancy

6

Conclusion

Will complete register and cache and associated chip characterization of the Motorola PowerPC 750 soon.

Verification that major important effects are now known should be attempted using well-analyzed "application-like" benchmarks.

Much has been accomplished, much remains to be done.

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 0: Welcome

Sammy Kayali

Advanced Microprocessor Radiation Testing Technical Peer Review

•The Remote Engineering and Exploration (REE) Project is evaluating the use of advanced commercial microprocessors for on-board data processing in spacecraft. One of the project's main thrusts has been radiation testing of the Power PC750 microprocessor, a high-performance processor with power dissipation of 6 Watts.

•The purpose of this review is to provide a critique of the results of the work completed at this point, along with the proposed direction of subsequent work planned for this fiscal year.

2

Key Objectives of the Peer Review

- Convene a group of qualified experts to review progress, technical quality, objectives and future direction for the study.
- Evaluate specific findings of the study, including the following areas:
 - (a) Test techniques and methods used for testing these complex devices
 - (b) Specific test results and data analysis methods
 - (c) Validity of the test results and methods of estimating error rates in space
- Provide a formal critique of the work that represents the consensus view of the review panel.
- Assess the feasibility of using acquired experimental test data in the development of effective fault tolerance methods and tools.

3

Requested Outputs

- Individual responses to evaluation form.
- Brief consensus summary report by the committee, coordinated by E-mail.
- Specific comments from individual review board members, as deemed necessary.

4

Outline

Overview of the REE Program	Rafi Some
Background	Allan Johnston
Test Approach	Gary Swift
Proton Test Results	Doug Millward
Test Methods	Gary Swift
Data Analysis Methods	Doug Millward
Heavy Ion Test Results	Steve Guertin
Proton/Heavy Ion Results Comparison	Larry Edmonds
Space Environments	Allan Johnston
REE Fault Model Overview	Arbi Karapetian
Error Rate Calculation	Larry Edmonds
Error Rate Results	Gary Swift
Conclusion and Near-Term Plans	Gary Swift

5

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 1: Overview of the REE Program

Rafi Some

REMOTE EXPLORATION AND EXPERIMENTATION (REE) PROJECT



Autonomous Robotic Vehicles



Deep Space Exploration



High Data Rate Instruments

Jet Propulsion Laboratory
California Institute of Technology

Project Manager: Robert Ferraro
Deputy Project Manager: Mukund Gangal

Project Scientist: James C. Ling

What is REE?

- REE is a technology project funded by NASA Code S for developing an onboard supercomputing capability for space applications.
- REE is one of five projects under the NASA HPCC Program. The other four projects are:
 - CAS - Computational Aerospace Sciences
 - ESS - Earth and Space Sciences
 - LT - Learning Technologies and
 - NREN - NASA Research and Educational Network
- The goal of REE is to use the state of the art commercial-of-the-shelf computer technology in space to significantly enhance the scientific objectives of the mission at a greatly reduced cost.
- REE will achieve onboard computing capability of >300 MOPS/watt scalable to mission requirements. The current RAD6000 (the state of the art radiation hardened microprocessor) single board computer operates at ~ 1 MOPS/watt.

NASA HPCC Project & Goals

REE (Remote Exploration and Experimentation): (1) Demonstrate a process for rapidly transferring commercial high performance computing technology into ultra-low power, fault tolerant architectures for space. (2) Demonstrate that high-performance onboard processing capability enables a new class of science investigation and high autonomous remote operation.

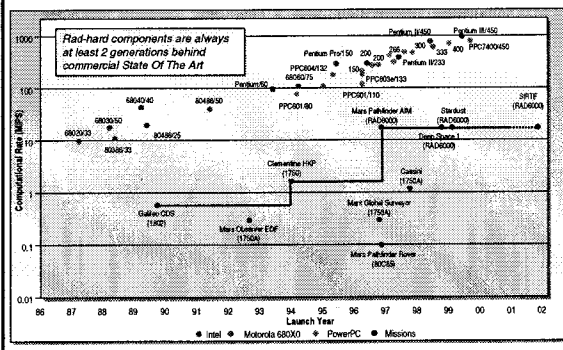
CAS (Computational Aerospace Sciences): Enable improvements to NASA technologies and capabilities in aerospace transportation through the development and application of high performance computing technologies and the infusion of these technologies into the NASA and National aerospace community.

ESS (Earth and Space Sciences): Demonstrate the power of high end and scalable cost effective computing environments to further our understanding and ability to predict the dynamic interaction of physical, chemical, and biological processes affecting the Earth, the solar-terrestrial environment, and the universe.

LT (Learning Technologies): To research and develop products and services that use NASA content and that facilitate the application of technology to enhance the educational process for formal and informal education and life long Learning.

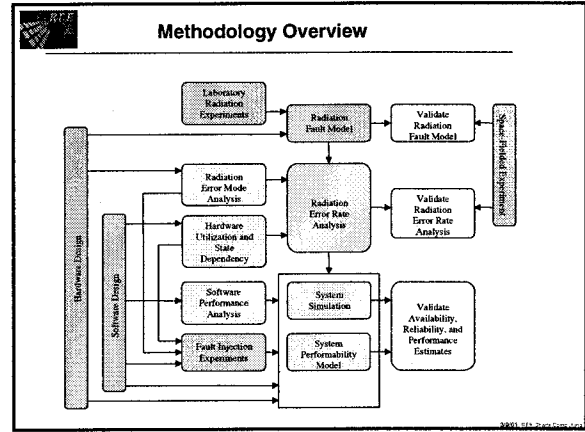
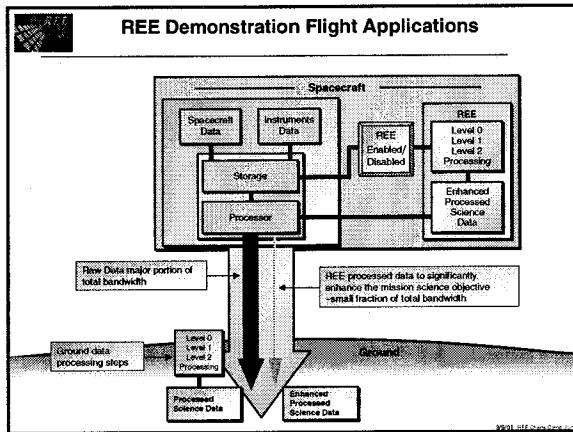
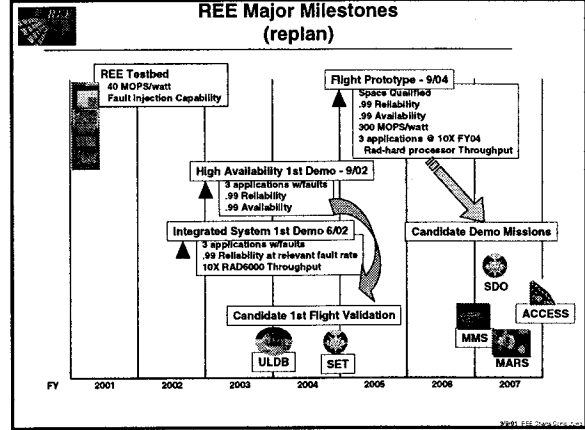
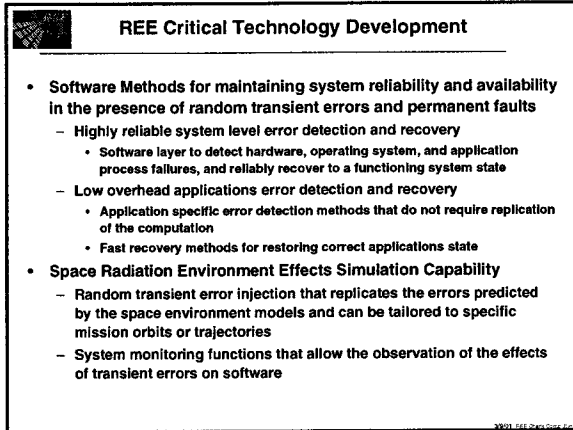
NREN (NASA Research and Educational Network): Extend U.S. technological leadership in computer communications through research and development that advances leading edge networking technology and services, then apply these enhanced capabilities to NASA mission and educational services.

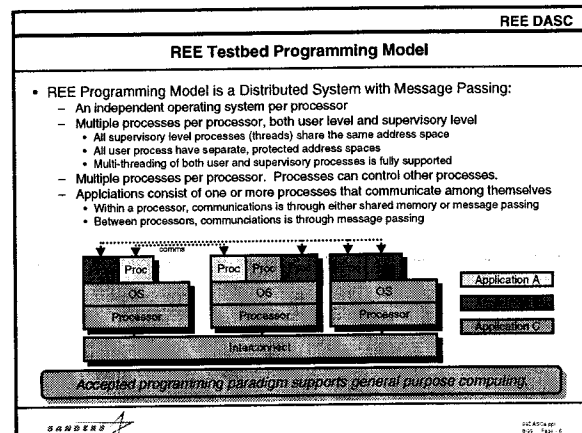
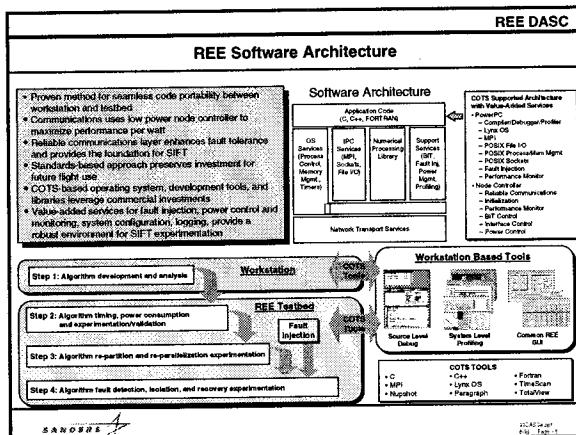
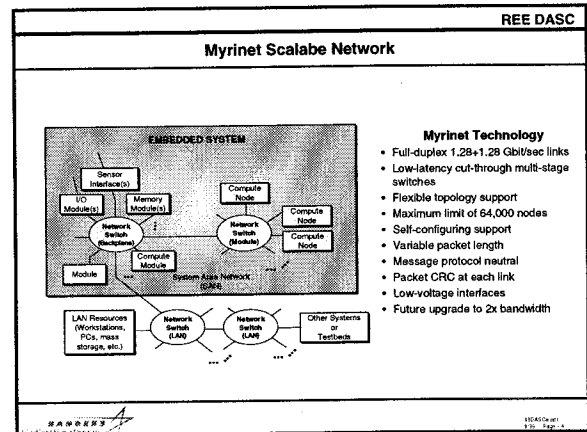
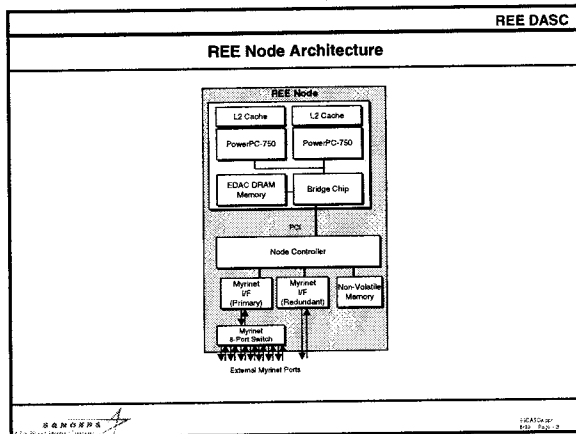
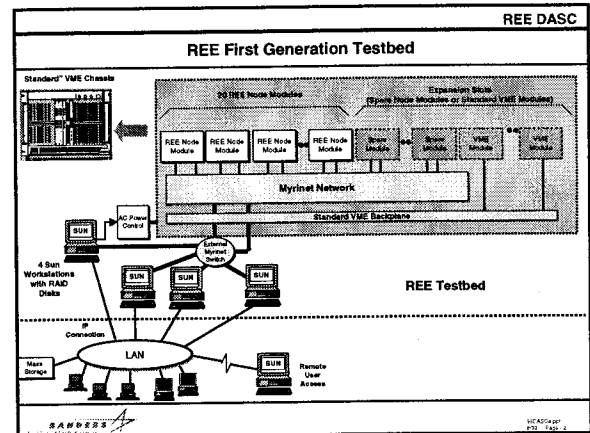
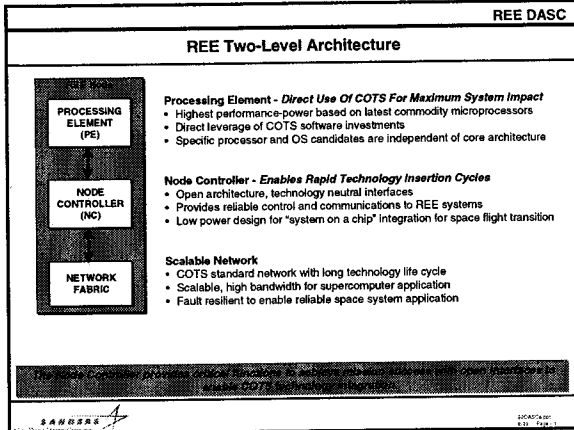
Space Flight Avionics & Microcomputer Processor History



REE Critical Technology Development

- Viability of COTS Hardware for Space Missions
 - Commercial Technology Family viability prediction
 - Characterizing commercial component technologies with respect to radiation hardness and susceptibility to single event effects to a level that allows modeling and prediction of their behavior in a space environment without exhaustive testing
 - Low cost hardware solutions to mitigating single event effects and attain mission life reliability
 - Memory organization, watchdog timers, fault tolerant controllers and interfaces for assembling COTS boards into a system
 - Low cost packaging and assembly methods for dealing with launch/landing shock & vibration, and in-space thermal management
 - Commercial components assume a convection cooling environment





REE DASC

Portable Application Programming Interfaces

- Portable Application Programming Interfaces:
 - MPI 1.2
 - Subset chosen for best value
 - Support multi-threaded processes
 - Support multiple independent processes
 - C, C++, and Fortran bindings
 - Demonstrate MPI-IO subset built on MPI
 - COTS OS
 - Standard Unix File I/O
 - Threads (Posix 1003.1c)
 - Sockets (Posix 1003.1g)
 - NFS and RPC
 - Process and Memory Management (Posix 1003.1)
 - Posix 1003.1b real-time extensions
 - Numerical Processing Library (COTS)

```

      graph TD
        APIs((Common APIs)) --> App[Application on Workstation]
        APIs --> REE[REE Testbed]
        App -- Recompile --> REE
      
```

Standards-based APIs facilitate the portability of applications.

11-04704-01
8.01 Page 1

REE DASC

Following Charts Were Not On The DASC Paper

11-04704-01
8.01 Page 1

REE DASC

Node Controller Hardware Fault Tolerance Support

Node startup support

- FPGA load time out
- StrongARM startup time out
- Auto node restart / shutdown

NC Processor support

- Illegal instruction interrupt
- Memory management unit
- System bus timeout watchdog
- Memory/PCI access protection
- Memory parity detection
- Sector CRC check on external NVM (SW)
- Watchdog timers

BIT control, health and status support facilities

- Facility for BIT control, fault logging, and reporting for node
- Facility for primary-redundant network interface enable and power control

11-04704-01
8.01 Page 1

REE DASC

Standard VME Chassis

11-04704-01
8.01 Page 10

REE DASC

REE Testbed Configuration

11-04704-01
8.01 Page 11

REE DASC

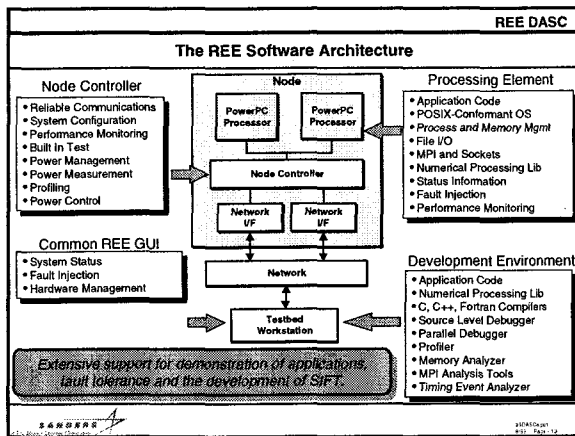
REE Software Architecture

Sun workstation

Node Controller

PPC 750

11-04704-01
8.01 Page 12



Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review
Section 2: Background
Allan Johnston

Outline

Earlier Approaches for Microprocessor Testing

- Register tests
- Application software
- "Golden" chip
- Watchdog timer to define hangs and crashes

General Testing Issues

- Operational conditions
- Error latency

Practical Testing Issues

- Flip-chip construction
- Power dissipation

Earlier Test Results

General Scaling Issues

2

Earlier Testing Approaches

Register-Level Testing

- Reduces results to familiar terms
- May be extended to real May 28, 2000
- Doesn't adequately test microprocessor core

Application Software

- Difficult to extend to other applications
- Results highly variable

Golden Chip

- Lockstep comparison
- Provides clock-cycle error visibility

3

Operating Systems

Machine Language

- No operating system
- Software development and monitoring difficult for advanced devices

Board-Level Operating System

- Primitive with minimum overhead
- Provides I/O, status and easy interfacing

Higher-Level Operating Systems

- Extremely complex
- Mask processor activity
- Very limited internal visibility

4

RAD6000 Processor

Version 0

- Hardened for total dose, but not for single-event upset
- SEU data on Version 1 from manufacturer used to calculate upset rates for Pathfinder

Version 1

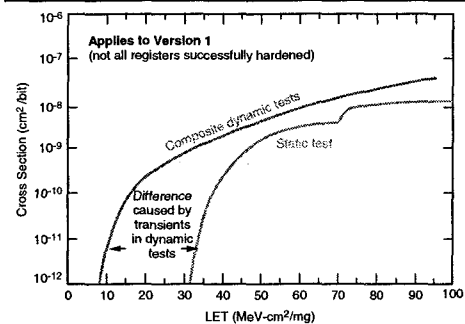
- This version flown on Pathfinder
- Hardened for single-event upset
 - Several internal registers were overlooked
 - Intermediate SEU hardness
 - One possible error in 9-month mission ("quiet" period)

Version 2

- Fixed oversights in Version 1
- Advertised register error rate 5.3×10^{-9} errors per bit-day

5

Radiation Test Results for RAD6000



6

Augmentation of Register-Level Testing

Status Monitoring

- Provides additional visibility
- Easily implemented

Adding Additional Processor Functions

- Cache
- Floating point operations

Watchdog Timer

7

Practical Testing Issues

Flip-Chip Bonding

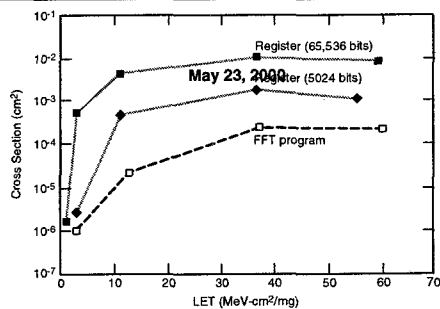
- Eliminates ability to "delid" device
- SEU testing still possible with extremely energetic ions
- Back irradiation provides an alternative approach
 - Mechanical "thinning" reduces range requirement
 - May not be equivalent to top irradiation
 - Thinning may alter device properties

Power Dissipation

- Power PC750 dissipates 6W at full speed
- Difficult issue in vacuum chamber
- Heating may be worse for thinned samples

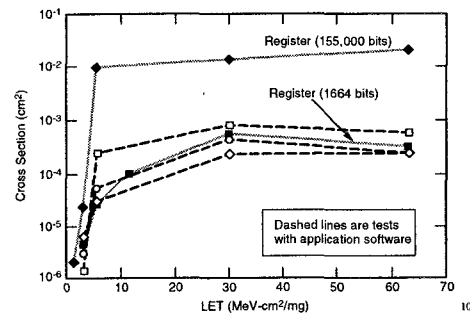
8

Single-Event Upset Results for PC603e



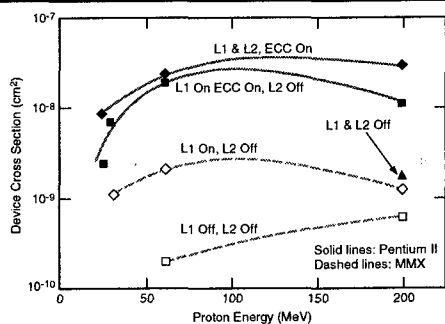
9

Single-Event Upset Results for Intel 486



10

Proton Upset Results for Advanced Intel Processors



11

Intel Processor Tests

Intended for Space Station Application

- Dominated by protons (no heavy ion testing done)
- Used high-level operating system

Two types of software

- DOS-based program
- NT-based program

Operating System "Crashes" Dominated

- Register error not observed in many of the runs
- Results difficult to compare with more basic tests

12

Other Considerations

Newer Processors Are More Complex

- Larger number of registers
- Cache memory nearly always used
- Increases *chip* error rate

Processors "Crash" Frequently During Radiation Testing

- Many possible operational failures
- Nearly impossible to categorize
- Crashes in applications may be difficult to deal with
 - Identification and latency
 - Recovery modes

Crashes Very Infrequent in Hardened Processors

13

Dealing with "Hangs"

"Hangs" Interfere with Error Rate Measurements

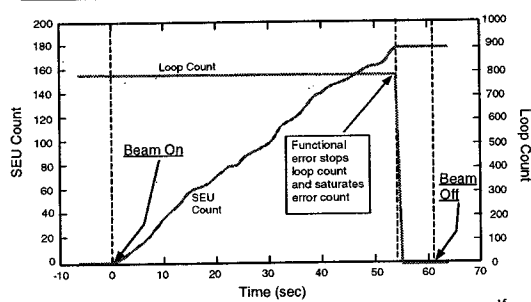
- Affect statistical uncertainty of measurements
- Difficult to categorize

Ways to Minimize Effect of "Hangs"

- Use very simple test algorithms
- Validate partial runs

14

"Strip Chart" Approach for Error Recognition



15

Other Considerations

SEU Rates in Commercial Processors Are Not Controlled

- SEU sensitivity and upset rate may change with manufacturing improvements (not a factor for hardened processors)

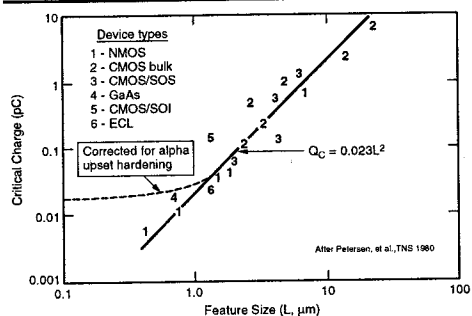
Frequent testing required for critical applications

Commercial Processors Appear Satisfactory for Non-Critical Data Processing

- Substantial risk if used for spacecraft control or critical data
- Error rates unacceptable during solar flares
- Processor crashes not thoroughly characterized
- Spacecraft control generally does not need processing speed of advanced devices

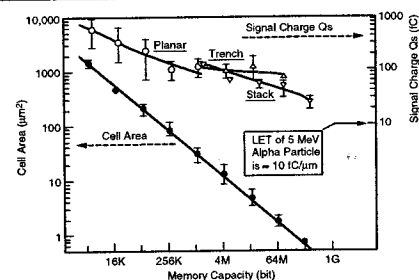
16

Device Scaling: Early Results by Petersen, et al.



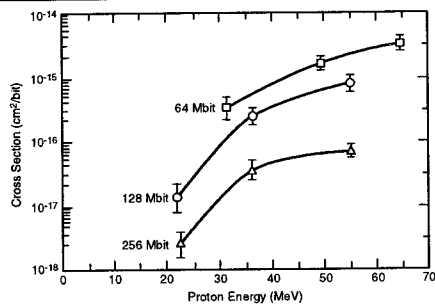
17

DRAM Scaling: Basic Design



18

DRAM Scaling: Proton Upset



19

Scaling Trends (after Davari)

Parameter	Late 1980's	1992	1995	1998	2001	2004
Supply voltage (V)						
High performance	5	5/3.3	3.3/2.5	2.5/1.8	1.5	1.2
Low power	-	3.3/2.5	2.5/1.5	1.5/1.2	1.0	1.0
Lithog. resolution (μm)	1.25	0.8	0.5	0.35	0.25	0.18
Channel length (μm)	0.9	0.6/0.45	0.35/0.25	0.2/0.15	0.1	0.07
Gate oxide thickness (nm)	23	15/12	9/7	6/5	3.5	2.5
Relative density	1.0	2.5	6.3	12.8	25	48
Relative speed						
High performance	1.0	1.4/2.0	2.7/3.4	4.2/5.1	7.2	9.6
Low power	-	1.0/1.6	2.0/2.4	3.2/3.5	4.5	7.2

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Microprocessor Scaling

Device	Manuf.	Year	Feature Size (approx.)	Threshold LET (MeV·cm²/mg)
Z-80	Zilog	1986	3 μm	1.5 - 2.5
8086	Intel	1986	1.5 μm	1.5 - 2.5
80386	Intel	1991	0.8 μm	2 - 3
68020	Mot.	1992	0.8 μm	1.5 - 2.5
LS64811	LSI	1993	1.2 μm	2 - 2.5
90C601	MHS	1993	1.2 μm	2 - 2.5
80386	Intel	1996	0.6 μm	2 - 3
PC603e	Mot.	1997	0.4 μm	1.7 - 3
Pentium	Intel	1997	0.35 μm	2 - 3
Power PC750	Mot.	2000	0.25 μm	2 - 2.5

21

Scaling for Microprocessors

Complex Problem with Several Competing Factors

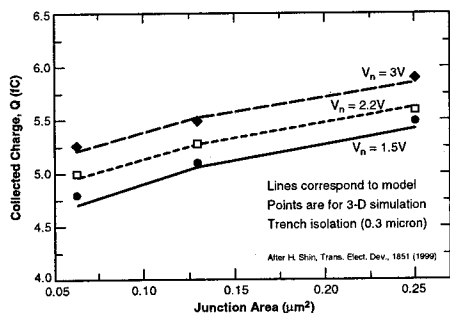
- Charge collection
- Critical charge
- Device area
- 3-D charge collection

Logic Transients Expected for Extreme Scaling

- Noise margin decreases as logic levels drop
- Threshold voltage doesn't scale
- Clock, logic design partially overcomes these limitations
 - Clock design is extremely complex
 - Corrects for skew; allows operation at extremely high speed
- Logic transients will likely increase processor upset rates to unacceptable levels

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DRAM 3-D Charge Modeling



23

Recommendations

Continue to Use Hardened Processors for Spacecraft Control and Critical Data

- RAD6000 is Proven Commodity
 - Reliable level of hardness in space - proven history
 - Does not require periodic testing and qualification
 - Free from strange error modes and crashes

Commercial Processors Attractive for Less Critical Use

- Higher speed, more processing power
- May be turned off or ignored during solar flares
- More work needed to evaluate operational integrity in applications
- Scaling effects may cause error rates to be worse for future generations
- Commercial operating systems introduce complications and higher error rates

24

08-29-1901 9.01√1
Processed: 4

Physical Inventory Worksheet
Pct Selected:100.0

TSCNBINM 7
Selected: 4

Trace	DtCd	Ext	St	D	Generic	Description/Lot Number	non-FL	FLIGHT	
OH033	8939		54	U	5962		0	0	[
	1)	A1-01	n		F				
OH034			54	U	27512		0	0	[
	1)	A1-01	n		F				
C3623	8224		78	U	54L10	9775144 NB	0	2	[
	1)	A1-01	n		F				
N0006	7829		78	C	CKR05	33pF 200V 10%	0	2	[
	1)	A1-01	n		F				

Report Directory: \USER\THERNAND

Continue(C),Restart/Reselect(R),End(E) C

Start Col# 1 Jet Propulsion Laboratory
Ctrl+Right/Left Arrow to Slide(5) Columns

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 3: Test Approach

Gary Swift

Outline

Philosophical Choices

- Register v. application testing
- "Golden chip" v. self-test
- Buy v. Build test platform

Overview of Approach Taken

- Static memory testing
- Pseudo-static processor testing

Other Considerations

- Use of JTAG boundary scan
- Validation of approach

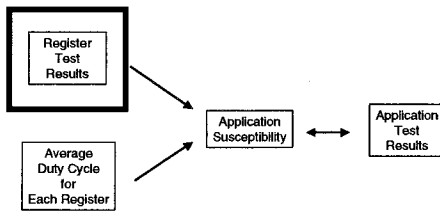
Generic Approach Alternative

- How it works
- Advantages and disadvantages

2

Register v. Application Tests

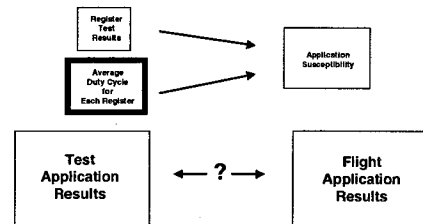
Register Testing Yields "Fundamental" Information



3

Register v. Application Tests

Calculation Of Space Upset Rates



4

Golden chip v. self tests

Finessed this by doing (almost) nothing during the beam

- One word infinite loop during beam- *HERE: Jump to HERE*
- User breaks out with "external interrupt"
- Self-inspection, if any, goes on out-of-beam
- Requires processor functionality post-beam
 - Reset or even power cycle may be okay
- Added half second snapshot stripchart in memory
 - Now "only" 99.9% in infinite loop

Does not preclude virtual golden chip testing later, as needed

5

Buy v. Build Considerations

Evaluation Board allows:

- Test at speed
- Quick to first test
- Adequate to build on (?)

Minimize efforts for Maximum Results

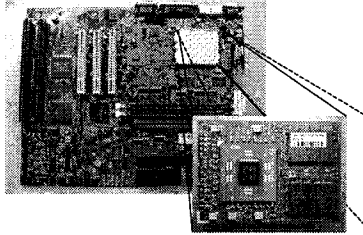
- Minimize custom hardware
- Minimize machine coding

Automate (and Maximize) Data Collection

Leverage Existing Rad Group Resources

6

"Yellowknife" Development Board with Processor/Cache Module (PCM)



7

Buy v. Build Considerations

Evaluation Board allows:

- Test at speed
- Quick to first test
- Adequate to build on (?)

Minimize efforts for Maximum Results

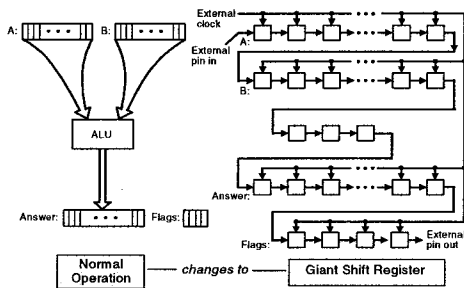
- Minimize custom hardware
- Minimize machine coding

Automate (and Maximize) Data Collection

Leverage Existing Rad Group Resources

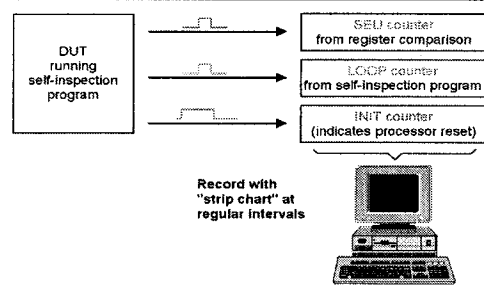
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Boundary Scan



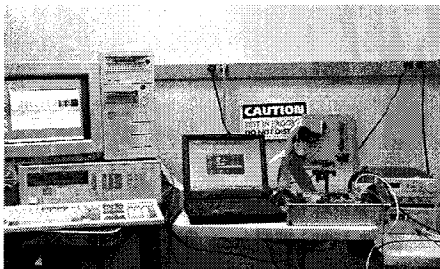
9

Overview of "Pin Wiggler" Method



10

Generic Test Approach: Pin Wiggler

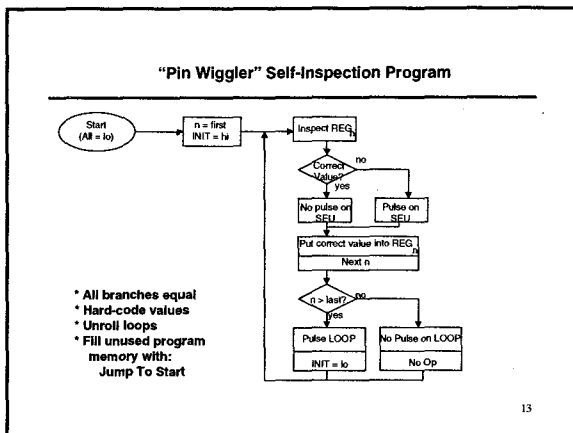


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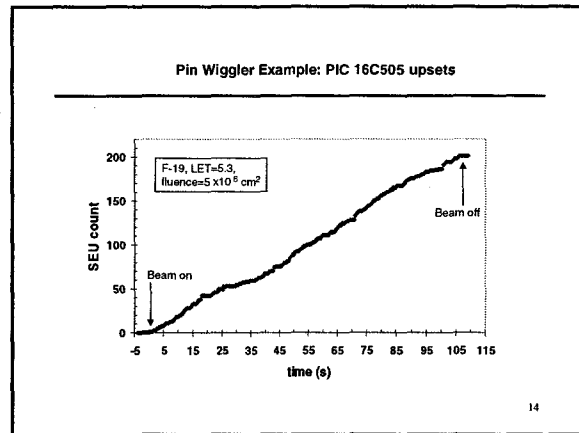
Generic Test Approach: Pin Wiggler



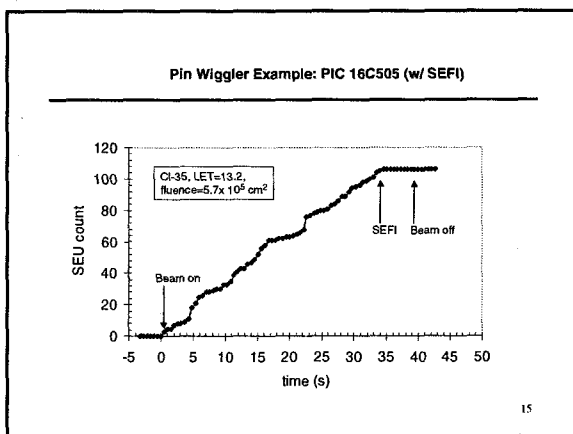
12



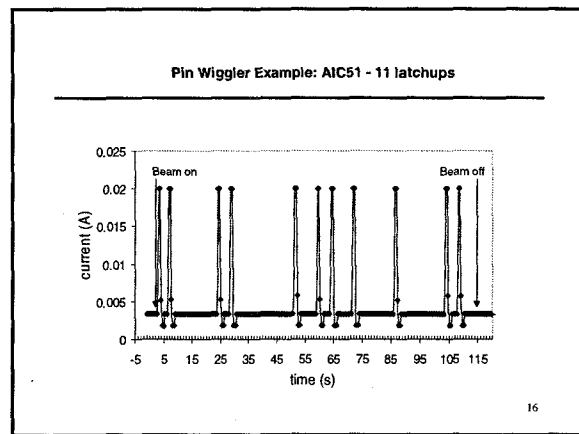
13



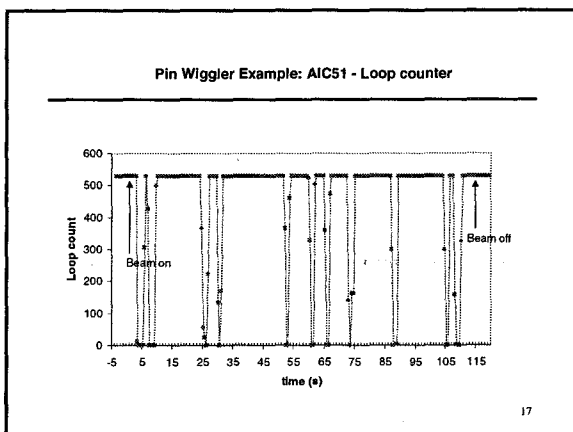
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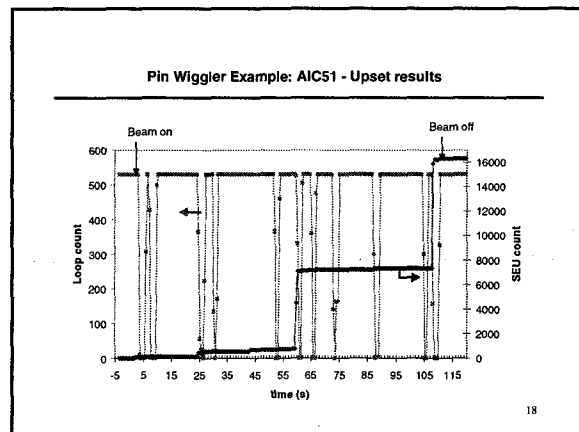
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17



18

Conclusion

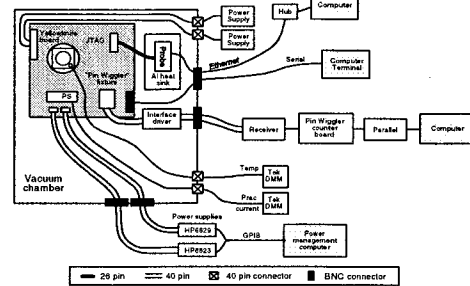
"Pin Wiggler" is:

- simple
- data rich

but has limitations of all register testing

19

Test Approach Using "Yellowknife" Development Board



20

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 4: Proton Test Results

Doug Millward

Outline

Introduction to Proton Testing

Test Facilities

- Indiana University Cyclotron Facility (IUCF)
- UC Davis Crocker Nuclear Laboratory (CNL)

Power PC 750 Proton SEU Data

- Registers (FPR, GPR, SPR)
- L1 Cache
- L1 Cache Tags/Flags

Discrepancy between facilities at 60-65 MeV

Comparison to earlier PowerPC 603e data

2

Introduction to Proton Tests on MPC750

- Proton tests more straightforward than heavy-ion tests.
 - Done in air rather than vacuum
 - Allow easy development and checkout of test hardware/software
 - Provide estimate of device behavior in subsequent HI tests
- Checkout of hardware/software in proton environment indicated significant effect of program "hangs".
 - In our tests, processor needs to run successfully to identify internal errors, therefore program "hangs" limit/negate data
 - Program modified to reduce effect of "hangs"
 - Software modified to minimize processor activity
 - Hardware and software simplified as much as possible
 - Test approach modified to mitigate effect of "hangs"
 - JTAG probe used to capture pre- and post-beam register contents
 - Strip Chart generated showing near real time register contents
 - Use of low-fluence runs produced good data with minimum "hangs"

3

Proton Facilities

Indiana University

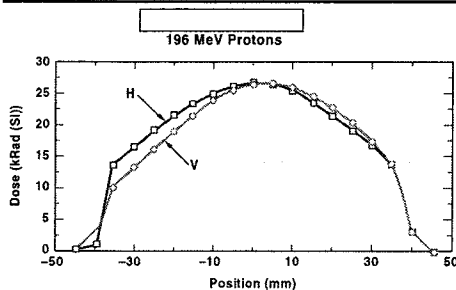
- "Raw beam" is 200 MeV
- Lower energies obtained by interposing Cu degraders
- Results in spread of energies, particularly with thick degraders
 - Up to 3.3 cm of copper used to degrade beam
 - Tests with 60-MeV degraded beam overlap maximum energy at Davis

UC Davis

- Beam is tuned to obtain nominal desired energy
- Tuned energies from 15 to 65 MeV
- Corrections for air, window losses, DUT thickness required at lowest energies

4

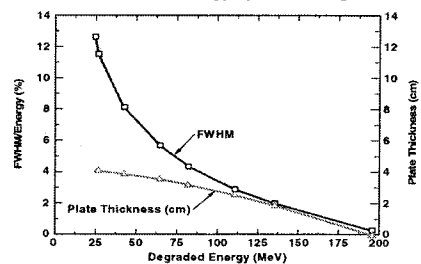
IUCF Beam Profile



5

Degrader Properties at IUCF

Plate Thickness and % Energy Spread vs Degraded Energy



6

Proton Test Results for MPC750

Registers Tested with Ones or Zeros Loaded

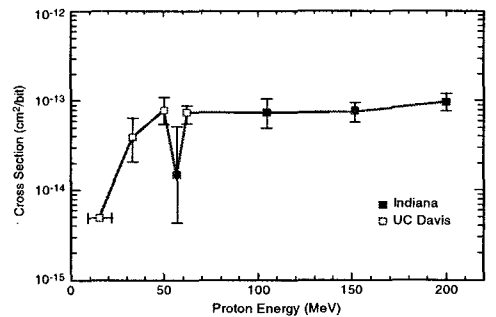
- Saturated cross section 10^{-13} cm²/bit for "1" to "0" transition
 - Cross section approximately three times lower for "0" to "1" transition
 - Explanation not known but probably due to differences in design of register cells and geometry of internal transistors
- Threshold between 30 and 50 MeV

D-Cache Tested with Ones or Zeros Loaded

- Saturated cross section about a factor of two lower than Registers
- Threshold below lowest energy used at UC Davis (~20 MeV)
- No significant differences observed between Ones or Zeros
- L1 Cache Tags/Flags behave in a similar manner to Cache
- Explanation based on use of small-area devices
 - Smaller saturated cross sections
 - Smaller Q_{crit} implies lower recoil energy deposition (from nuclear interaction) needed to produce upset

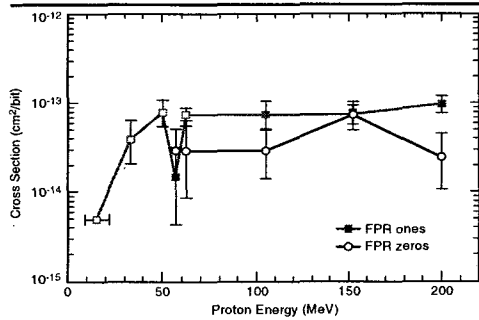
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Upset Cross Section for FP Registers ("1" transitions)



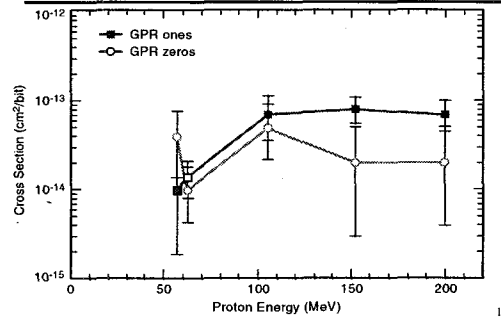
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Upset Cross Section for FP Registers (both transitions)



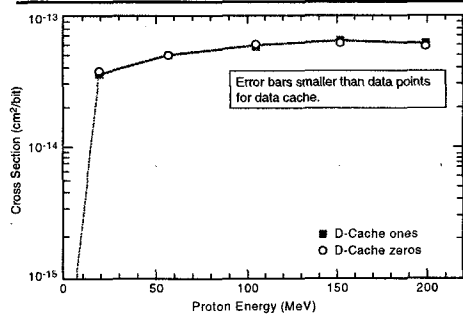
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Upset Rates for General-Purpose Registers



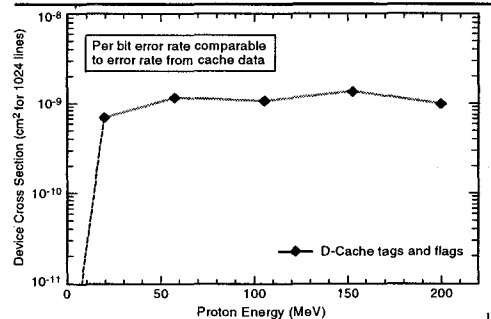
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Proton Cross Section for Data Cache



11

Proton Cross Section for D-Cache Tags and Flags



12

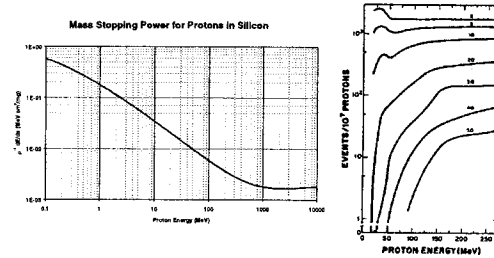
Discrepancy Observed at 60-65 MeV

Differences seen in SEU cross sections between IUCF and UC Davis at 60-65 MeV

- σ_{IUCF} approximately five times less than σ_{UCD} at 60-65 MeV
- Possible explanations include:
 - Low-energy contamination of IUCF beam
 - Energy spectroscopy would determine amount of low-energy protons present
 - Poisson statistics
 - Error in Cu degrader thickness
 - Measurement errors

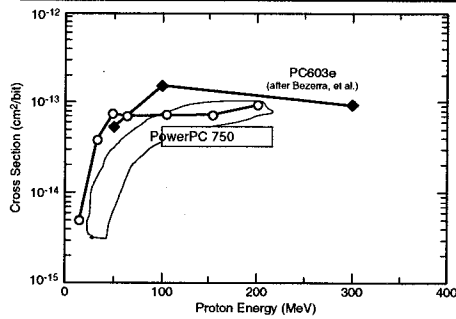
13

Energy Dependence of Proton dE/dx (Dose) and Proton SEU Error Rate (Nuclear Reaction σ)



14

Comparison of Proton SEU Cross Sections for PowerPC750 and PC603e



15

Summary and Conclusions

Initial experiments performed at proton facilities allowed checkout of test approach and modification of hardware and software in simple particle environment.

Discrepancy has been noted between SEU cross section measured at IUCF and UC Davis.

Upset susceptibility of MPC750 registers is 3x higher when storing 1's relative to storing 0's. Energy threshold is ~15 MeV.

Upset susceptibility of L1 data cache bits is symmetric, and the energy threshold is below 15 MeV.

Upset of L1 cache Tags/Flags remarkably similar to L1 cache data bits.

16

Gary Swift

- PowerPC Family and 750 Architecture
- Test Chronology
- Degrading Heavy Ions for LET Coverage
- Details of Test Approach
- Dealing with Test Problems

2

[illegible]

3

[illegible]

4

Abbreviations	Description	# of bits
GPR	General Purpose Registers	1024
FPR	Floating Point Registers	2048
SR-SPR	Special Purpose Registers	2560
Data Cache Data Bits	Self-explanatory	256K
Data Cache Tags & Flag	Cache Addresses	20K
Instruction Cache Data Bits	Self-explanatory	256K
Instruction Cache Tags & Flag	Cache Addresses	20K
TLBs	Page Table Cache	1024 lines
L2 Cache Tags & Flag	L2 Cache Addresses	40K

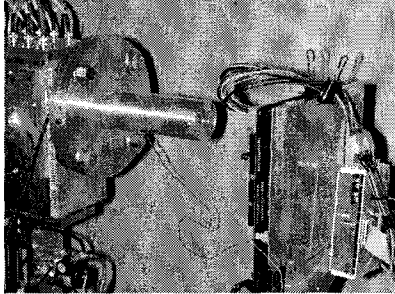
5

Test #	Date	Facility	Beam
1	Dec. 1999	UCF	60 - 200 MeV protons
2	Apr. 2000	UCD	20 - 63 MeV protons
3	May 2000	UCD	20 - 63 protons
4	June 2000	TAM	long-range heavy ions
5	June 2000	UCF	60 - 200 MeV protons
6	July 2000	TAM	long-range heavy ions

IUCF = Indiana University Cyclotron Facility, Bloomington, IN
UCD = University of California at Davis
TAM = Texas A & M University Cyclotron, College Station, TX

6

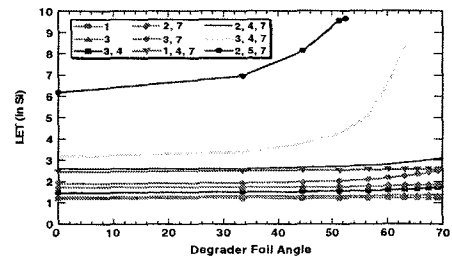
TAM In-Air Irradiation Facility



7

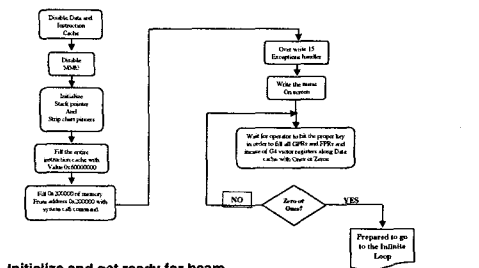
Degrading Ne LET at Texas A&M

LET (in Si) vs. Degradation Foil Angle for ^{20}Ne (40MeV/amu)



8

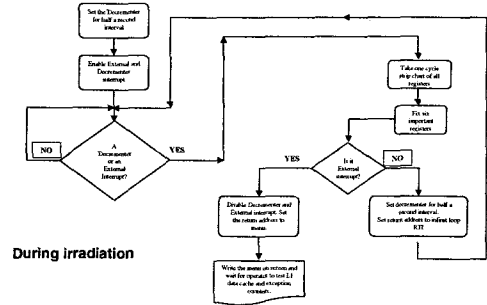
Test Program



Initialize and get ready for beam

9

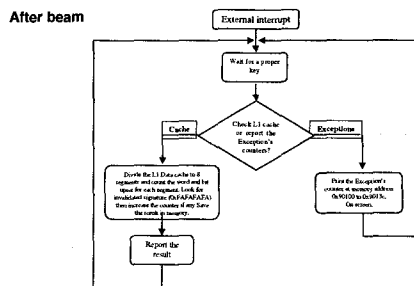
Test Program (cont.)



During irradiation

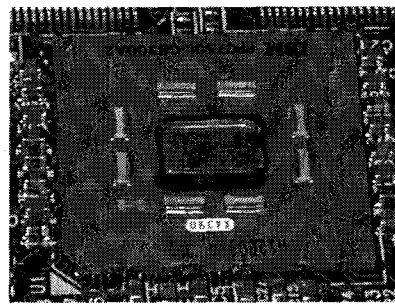
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Test Program (cont.)



11

A Thinned IBM PowerPC 750



12

Dealing with "Hangs"

"Hangs" Interfere with Error Rate Measurements

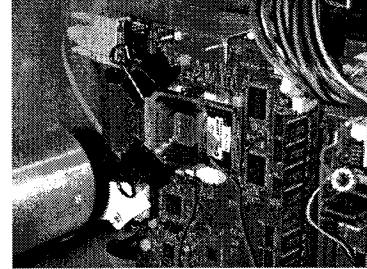
- Affect statistical uncertainty of measurements
- Difficult to categorize

Ways to Minimize Effect of "Hangs"

- Use very simple test algorithms
- Validate partial runs

13

Dealing with Thermal Problems



14

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 7: Heavy Ion Results

Steve Guertin

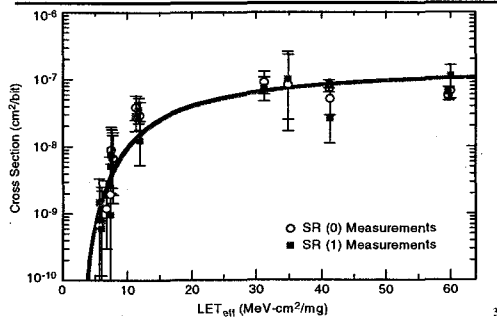
Outline

- Specific Register Results
- Cache Results
- Processor Comparison
- Concluding Remarks

2

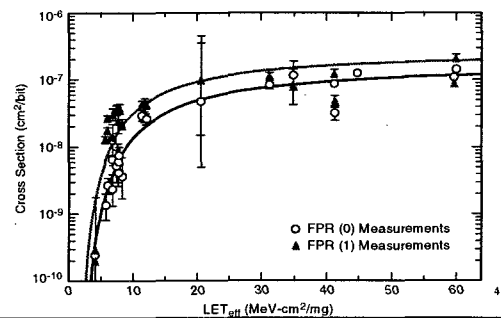
SEU Cross Section for Special Purpose Registers

(note: Low LET results mostly "pin wiggler" data)



3

SEU Cross Section for Floating-Point Registers



4

Practical Testing Issues

Flip-Chip Bonding

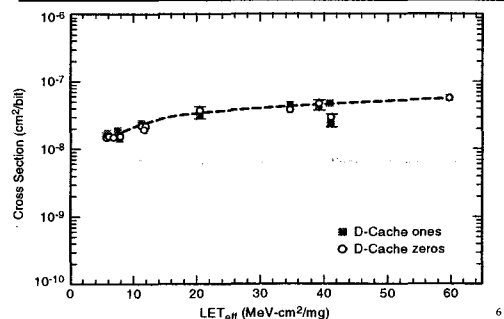
- Eliminates ability to "delid" device
- SEU testing still possible with extremely energetic ions
- Back irradiation provides an alternative approach
 - Mechanical "thinning" reduces range requirement
 - May not be equivalent to top irradiation

Power Dissipation

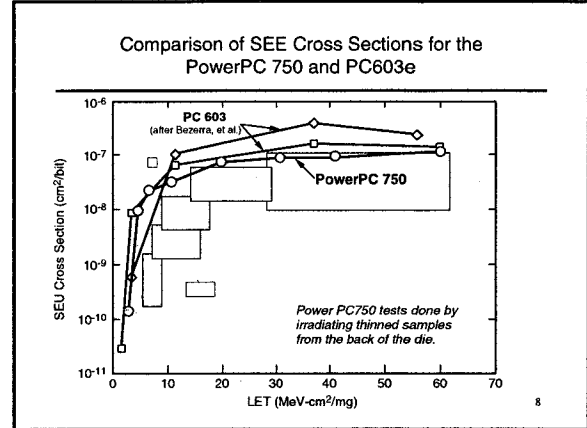
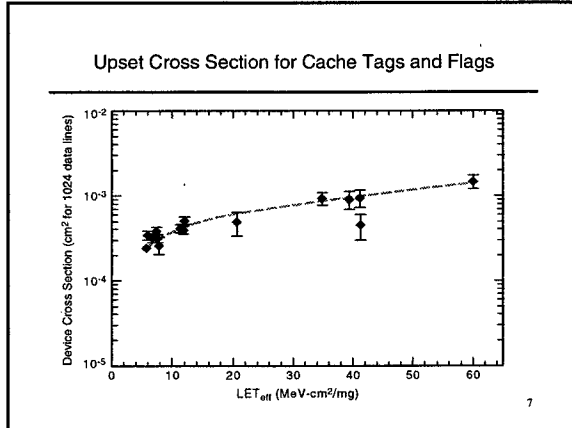
- Power PC750 dissipates 6W at full speed
- Difficult issue in vacuum chamber
- Heating may be worse for thinned samples

5

Upset Cross Section for Data Cache



6



Conclusions

- Registers storing 1's are more susceptible than those storing 0's.
This is consistent with the proton results.
- Cache bits are equally susceptible whether storing 1's or 0's.
This is also consistent with the proton results.
- The L1 data cache tags and flag are roughly the same susceptibility as the cache bits themselves. At this time, the testing does not separate the susceptibility of 1's and 0's.

9

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 8: Proton/Heavy Ion Results Comparison

Larry Edmonds

Outline

- Introduction
- Model for Obtaining Proton Results from Heavy Ion Data
- Model Results vs. Published Data
- PowerPC Results of the Model
- Conclusions

2

New Work Compared to Previous Work on the Proton/ Heavy Ion Relationship

All results previously derived from physical analysis (as opposed to empirical fits):

- Assume the RPP model
- Require supplemental information (RPP thickness or critical charge) in addition to heavy ion data for predicting proton cross sections.

New Work:

- Uses a more realistic physical model (a continuous charge-collection efficiency function instead of RPPs)
- Gives upper bound proton cross section estimates derived from heavy ion data (no supplemental information or fitting parameters required.)

3

A Relationship from Charge Collection Physics

Equation:

$$\sigma_{pr}(E) \leq \frac{\beta(E)}{a} \int_0^{\infty} \frac{1}{L} \frac{d\sigma_{hi}(L)}{dL} dL$$

where a is a constant and $\beta(E)$ is from a table

From:
L.D. Edmonds, "Proton SEU Cross Sections Derived from Heavy-Ion Test Data,"
IEEE Trans. Nucl. Sci., vol. 47, no. 5, pp. 1713-1728, Oct. 2000.

4

Comparison with Published SEU Results

PART	DATA	MODEL	RATIO
	$\sigma_{hi} (cm^2)$	$\sigma_{pr} (cm^2)$	
SMJ44100	7.0E-7	1.9E-6	2.7
6226R	1.5E-7	3.8E-7	2.6
IBM 16MEG	2.1E-8	5.8E-8	2.7
MT4C1004C	3.9E-7	1.0E-6	2.5
KM41C4000Z-8	3.3E-7	8.9E-7	2.7
O1G9274	4.2E-9	3.1E-8	7.4
OW 62256	8.7E-8	2.3E-7	2.6
MT4C4001	2.9E-7	1.2E-6	4.1
HM6116	4.6E-8	4.7E-8	1.0
62832H	2.9E-8	5.0E-8	1.7
2901B	8.5E-10	2.1E-9	2.5
TCS14100Z-10	1.0E-6	2.0E-6	2.0
HM 65656	3.0E-8	9.0E-8	3.2
M8814100 10PSZ	6.9E-7	2.9E-6	4.2
HY8514100J	1.5E-6	2.5E-6	1.7
LuNe C	2.1E-8	8.2E-8	3.9
D424100V-80	1.9E-8	2.3E-8	1.3
HM6515	2.5E-9	1.6E-8	6.5

5

Comparison with Published Results (cont'd)

SEU (per bit):

PART	DATA	MODEL	RATIO
	$\sigma_{hi} (cm^2)$	$\sigma_{pr} (cm^2)$	
Fairchild 93L422 (bipolar)	1.4E-10	9.8E-11	0.70
Samsung 16Mb 3.3V DRAM	3.5E-14	7.4E-14	2.1
Hitachi 16Mb 3.3V DRAM	1.8E-14	2.4E-14	1.5
Micron 16Mb 3.3V DRAM	8.0E-15	1.9E-14	2.3
IBM 16Mb 3.3V DRAM	1.7E-15	2.8E-15	1.6

Latchup:

PART	DATA	MODEL	RATIO
	$\sigma_{hi} (cm^2)$	$\sigma_{pr} (cm^2)$	
AMD K5 microprocessor	5.6E-9	1.9E-8	3.4
HM65162 (1985)	1.4E-10	2.9E-9	210

6

Checking PowerPC 750 Results

Registers were tested with both protons and heavy ions.

- Proton data at energies up to 51 MeV show the shape of the curve well enough to extrapolate. Extrapolating gives a saturation cross section of $\sim 1 \times 10^{-13} \text{ cm}^2/\text{bit}$.
- Heavy ion data used with the model predicts a proton saturation cross section of $1.3 \times 10^{-13} \text{ cm}^2/\text{bit}$ for the registers.

7

Conclusions

The upper bound estimate for the proton cross section is very nearly equal to the actual cross section measured for the PowerPC 750 registers.

8

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 9: Space Environments

Allan Johnston

Outline

• Introduction

• Model Environments for REE

- How Rates Are Calculated
- Rate Results
- Conclusions

2

Coming Attractions

REE Fault Model Overview	Arbi Karapetian
Error Rate Calculation	Larry Edmonds
Error Rate Results	Gary Swift
Conclusion and Near-Term Plans	Gary Swift
Discussion	Reviewers

3

Specific Missions Considered for REE Applications

Deep Space

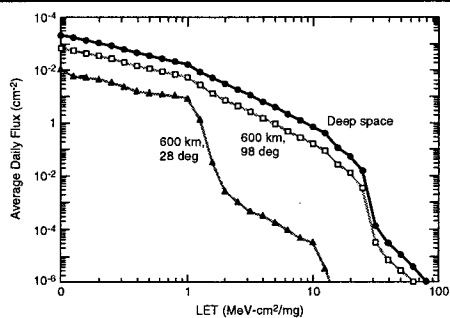
Surface of Mars

600 km, 98° Polar Orbit

600 km, 28° Polar Orbit

4

Galactic Cosmic Ray Spectra for Different Environments



5

Solar Flares

- JPL Uses a Specific Flare for Design Purposes
- GCR fluence approximately 1/10 that of October 1989 flare
 - Exponential time model ($\tau = 20$ hours)

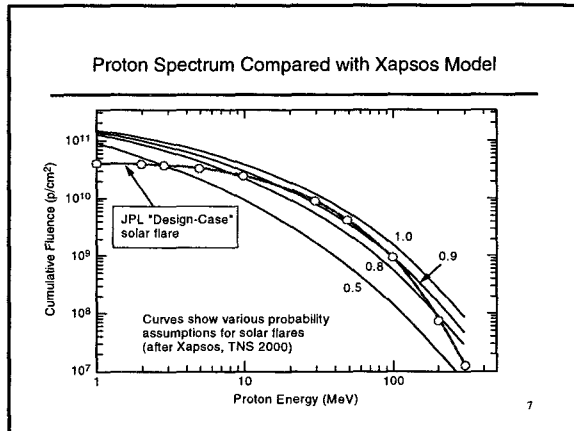
Proton Fluence

- Total fluence = $\times 10^{15}$ p/cm² (> 30 MeV)
- Corresponds to $P = 0.1$ on Xapsos probability model

Error Rates Calculated on Basis of 24-Hour Day

- Peak error rates during the first few hours of a flare are higher
- Conventional SEE rates usually reported in errors/bit-day

6



Radiation Evaluation of the PowerPC 750
Microprocessor

External Peer Review

Section 10: Overview of the Fault Model

Arbi Karapetian

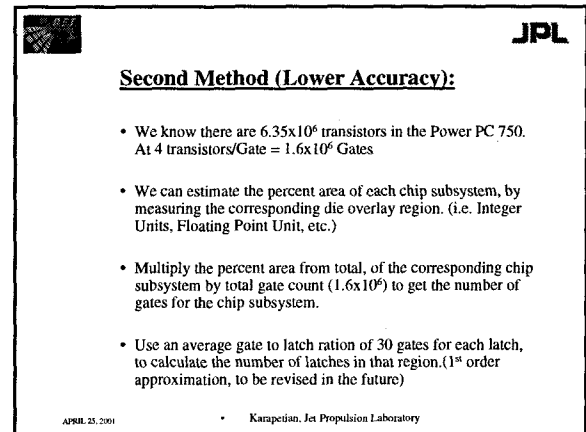
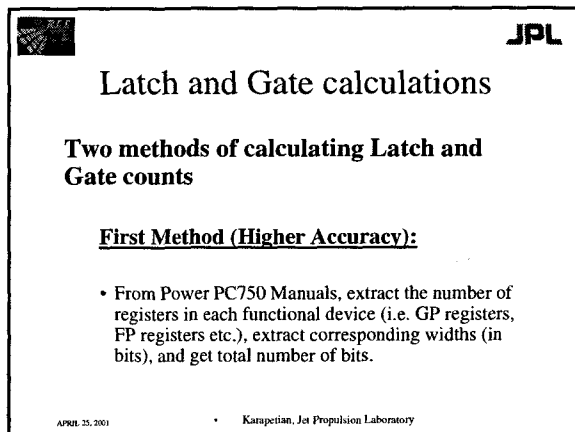
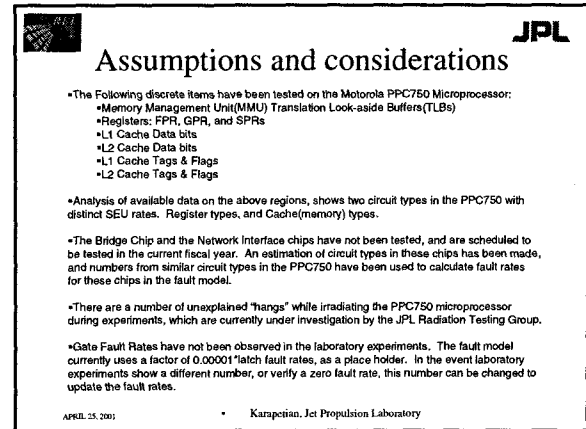
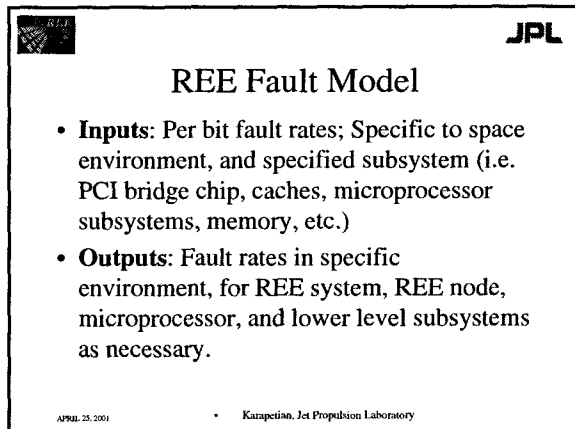
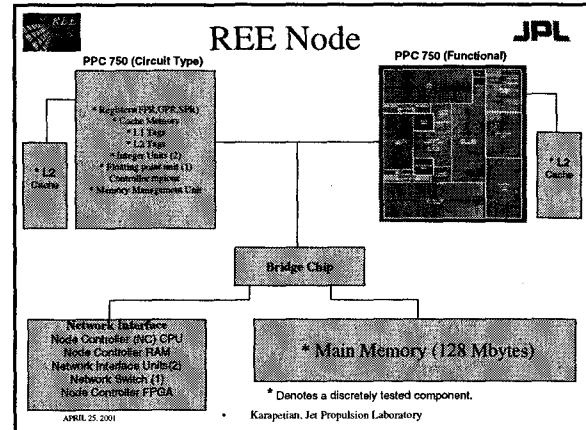
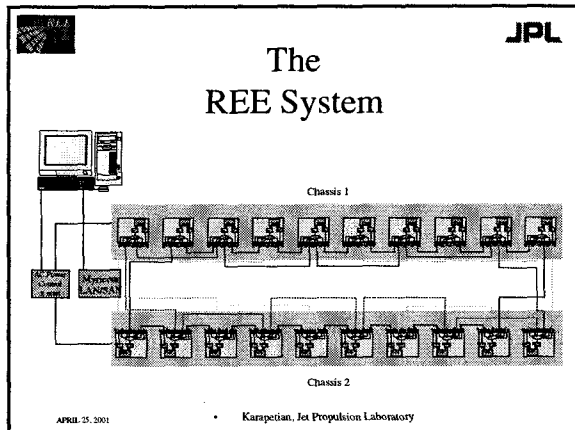
Outline

Overview of the Fault Model

Inputs and Outputs

Fault Model Results

2



Why have the fault Model?

- The fault model results will be verified against radiation experiments in laboratory radiation experiments of the system, and flight experiments, in order to validate the results.
- To estimate fault rates, for devices which are not accessible directly, or have not yet been tested.
- To extrapolate fault rates, for next generation processors.

APRIL 25, 2001
Karapetian, Jet Propulsion Laboratory

Sample calculation sheet for latch faults (First Method)

Item	Value	Unit	Value	Unit	Value	Unit
Gate count	1587500					
Gate fault rate (GFR)	9.54E-12					
Est. Latch	33760.8	% Area	100		1587500	1.514E-05
Instruction sequencer	8360.93	15.8	1587500	250825	9.54E-12	2.393E-06
Integer units	4127.5	7.8	1587500	123825	9.54E-12	1.181E-06
Floating point unit	5503.33	10.4	1587500	165100	9.54E-12	1.575E-06
Load/store unit	4286.25	8.1	1587500	128587.5	9.54E-12	1.227E-06
L1 D-cache	10.6	different density	1587500	168275	9.54E-12	1.605E-06
L1 I-cache	13.1	different density	1587500	207962.5	9.54E-12	1.984E-06
Dtags	2	different density	1587500	31750	9.54E-12	3.029E-07
Itags	2	different density	1587500	31750	9.54E-12	3.029E-07
L1 D-cache control	1217.06	2.3	1587500	36512.5	9.54E-12	3.463E-07
L1 I-cache control	793.75	1.5	1587500	23812.5	9.54E-12	2.272E-07
MMU TLBs	1.3	different density	1587500	20637.5	9.54E-12	1.969E-07
IMMU TLBs	1.3	different density	1587500	20637.5	9.54E-12	1.969E-07
L2 cache tags	5.9	different density	1587500	93662.5	9.54E-12	8.935E-07
L2 cache control and bus VI	3280.63	6.2	1587500	98425	9.54E-12	9.39E-07
PLL	476.25	0.9	1587500	14287.5	9.54E-12	1.363E-07
TAU	264.583	0.5	1587500	7937.5	9.54E-12	7.572E-08
unknown	5450.42	10.3	1587500	163512.5	9.54E-12	1.56E-06

APRIL 25, 2001
Karapetian, Jet Propulsion Laboratory

Sample calculation sheet for Gate Faults (Second Method)

Item	Value	Unit	Value	Unit	Value	Unit
Gate count	1587500					
Gate fault rate (GFR)	9.54E-12					
Est. Latch	33760.8	% Area	100		1587500	1.514E-05
Instruction sequencer	8360.93	15.8	1587500	250825	9.54E-12	2.393E-06
Integer units	4127.5	7.8	1587500	123825	9.54E-12	1.181E-06
Floating point unit	5503.33	10.4	1587500	165100	9.54E-12	1.575E-06
Load/store unit	4286.25	8.1	1587500	128587.5	9.54E-12	1.227E-06
L1 D-cache	10.6	different density	1587500	168275	9.54E-12	1.605E-06
L1 I-cache	13.1	different density	1587500	207962.5	9.54E-12	1.984E-06
Dtags	2	different density	1587500	31750	9.54E-12	3.029E-07
Itags	2	different density	1587500	31750	9.54E-12	3.029E-07
L1 D-cache control	1217.06	2.3	1587500	36512.5	9.54E-12	3.463E-07
L1 I-cache control	793.75	1.5	1587500	23812.5	9.54E-12	2.272E-07
MMU TLBs	1.3	different density	1587500	20637.5	9.54E-12	1.969E-07
IMMU TLBs	1.3	different density	1587500	20637.5	9.54E-12	1.969E-07
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L2 cache control and bus VI	3280.63	6.2	1587500	98425	9.54E-12	9.39E-07
PLL	476.25	0.9	1587500	14287.5	9.54E-12	1.363E-07
TAU	264.583	0.5	1587500	7937.5	9.54E-12	7.572E-08
unknown	5450.42	10.3	1587500	163512.5	9.54E-12	1.56E-06

APRIL 25, 2001
Karapetian, Jet Propulsion Laboratory

Fault Model Results

Average Rates (Fault/Hour)

	Mars Surface	Earth Orbit (600Km-28")	Interplanetary Space (Solar Minimum)	Interplanetary Space (Solar Maximum)	Interplanetary Space (Solar Min. w/Flare)
Single REE Node (100 Mil Al Shielding)	0.02	0.21	0.25	0.07	192.4
20 Node REE System (100 Mil Al shielding)	.34	4.14	4.97	1.33	3852.98

Environmental SEU rates per bit From Radiation Tests (specific to circuit type)

X

Number of bits in each functional block (Specific to circuit type)

=

Total Fault Rate in Specified Environment Per functional block

REE Node Fault Rate in Specified Environment

=

Sum of Fault Rates in Specified Environment Per functional block

APRIL 25, 2001
Karapetian, Jet Propulsion Laboratory

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review
Section 11: Error Rate Calculations
Larry Edmonds

Outline

- Introduction
- Model Environments for REE
- **How Rates Are Calculated**
- Rate Results
- Conclusions

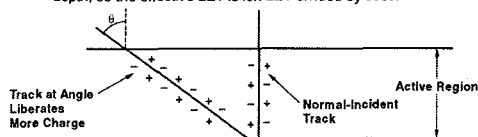
2

SEU Rate Depends on How Cross Section Varies with Both Ion LET and Incident Angle

Cosine law is usually assumed when plotting test data.

- Applies when active regions are thin enough so that lateral variations in the charge-collection efficiency can be ignored when comparing two points on the same track.

- The relevant quantity is liberated charge per perpendicular depth, so the effective LET is ion LET divided by $\cos\theta$.



3

SEU Rate Depends on How Cross Section Varies with Both Ion LET and Incident Angle (cont.)

- Often an adequate approximation for suitably restricted tilt angles.

But the active region is not always thin enough for lateral variations in the charge-collection efficiency to be unimportant, so the cosine law has limitations.

- Should always fail at some sufficiently large tilt angle.
- Sometimes fails even at small angles.

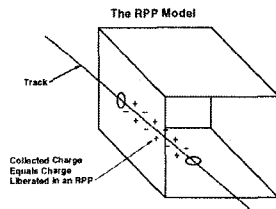
Therefore, a more versatile model is needed for SEU rates.

4

The RPP Model

The traditional model is the RPP model. It assumes that:

- Charge collected at a device node is the charge liberated within an associated RPP.



5

The RPP Model (cont.)

- A device contains a collection of geometrically identical RPPs but with different susceptibilities, i.e., different critical charges that collected charge must exceed for an upset.

- The gradual increase in a device cross section curve with increasing LET is from an increasing number of contributing RPPs.

6

Physics Doesn't Matter Because the RPP Model is Just a Fit

The assumptions behind the RPP model are not physically correct.

- Charge collected from ionization at a given location varies continuously as the location is varied.
- The increase in device cross section with increasing LET is largely, if not almost entirely, from an increase in each bit cross section, as opposed to an increase in the number of contributing bits.
- In particular, the physical assumptions behind the RPP model do not predict multiple bit upsets from charge sharing.

The assumptions don't have to be correct because use of the model is analogous to curve fitting.

7

Physics Doesn't Matter Because the RPP Model is Just a Fit (cont.)

The only requirement is that the dependence of cross section on LET and direction be correctly described.

The goal is to select model parameters that will produce a fit to measured data.

- A perfect fit to the normal-incident cross section versus LET curve can be obtained by selecting an appropriate distribution of critical charges.
- The directional dependence of the cross section is another issue.

8

Directional Dependence Implied by the RPP Model

The parameter describing the directional dependence is the ratio R of lateral dimensions to thickness (the two lateral dimensions are usually assumed to be equal).

- Very large R gives the cosine law.
- $R=1$ approximates an isotropic cross section.
- $R=5$ approximates the cosine law up to about 60° , with progressively larger deviations from the cosine law at larger angles.

The objective is to select the R that best describes the directional dependence (either measured or assumed) for the device considered.

9

A Source of Error

The RPP thickness need not be the dimension of any physical structure.

Therefore, the appropriate R should be determined from knowledge of the directional dependence of device cross section.

Unfortunately, test-ion range limitations prohibits testing at large angles, so there is almost always some uncertainty in the directional dependence.

10

A Source of Error (cont.)

Unfortunately, predicted SEU rates for hard devices are very sensitive to the assumed directional dependence.

• For example, one assumption regarding the directional dependence may predict that a hard device is completely immune to iron, while another assumption predicts upsets from hits by iron at sufficiently large angles.

• The two assumptions predict very different SEU rates.

Fortunately, predicted SEU rates for soft devices are less sensitive to the assumed directional dependence (e.g., all assumptions agree that hits by iron, at any angle, will upset very soft parts).

11

For The PowerPC 750 Case...

• All PC750 tests were at normal or near-normal incidence, so there is no indication of the directional dependence. But the device is soft enough so that predicted SEU rates are fairly insensitive to R .

• In the absence of conflicting information, we sometimes use $R=5$ as a best guess.

• A worst-case R is a trial-and-error selection to obtain the largest calculated rate (almost always produces the cosine law).

• Rates calculated from the two above R 's differ by about a factor of two (or less, depending on the environment) for the PC750.

• Close enough to not warrant additional investigation. The $R=5$ rates were chosen.

• However, additional tests at angles might show that the estimates are too conservative (e.g., if the cross section is nearly isotropic). This might be a motivation for additional tests.

12

A Caveat...

The D Cache data do not extend to low enough LET to show the shape of the cross section curve. Some modeling was used.

The cross section curve was described by a two-parameter curve (from diffusion theory) [1] instead of the four-parameter Weibull function because:

- The former curve was derived from charge transport physics while the Weibull function was not.

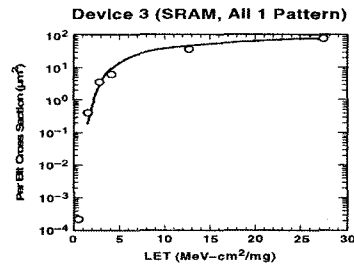
- If: The device cross section is the sum of cell cross sections i.e., tests count upsets instead of upset clusters when there are multiple-bit upsets.

And: Data are free of cosine-law errors.

Then: Data do not saturate as fast as the Weibull function, and fit the two-parameter curve better.

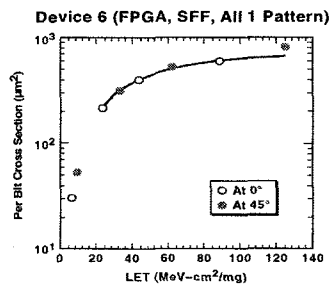
13

New Model Fit Example



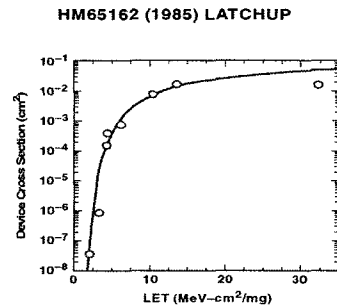
14

New Model Fit Example



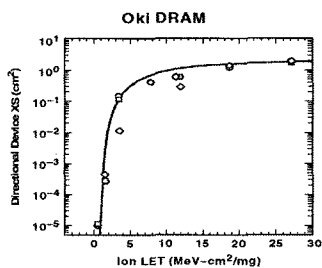
15

New Model Fit Example



16

New Model Fit Example



17

A Caveat... (cont.)

The two parameters were selected to:

- Fit the available heavy-ion data.
- Make the proton cross section derived from heavy-ion data [2] agree with the measured proton cross section.

Real data would be better.

- Predicted rate is sensitive to the way the data are extrapolated to lower LET.
- Calculated rate could be too small.
- Additional testing is needed.

[1] L.D. Edmonds, "SEU Cross Sections Derived from a Diffusion Analysis," *IEEE Trans. Nucl. Sci.*, vol. 43, no. 6, pp. 3207-3217, Dec. 1996.
 [2] L.D. Edmonds, "Proton SEU Cross Sections Derived from Heavy-Ion Test Data," *IEEE Trans. Nucl. Sci.*, vol. 47, no. 5, pp. 1713-1728, Oct. 2000.

18

Proton Rates

Cross section for protons is assumed to be isotropic, so proton rates are calculated by simply integrating the cross section (a function of proton energy) with the proton spectrum.

Rates from trapped protons dominate rates from heavy ions at low latitudes.

- Geomagnetic shielding attenuates the heavy ion spectrum.
- Severe proton environment during passes through the South Atlantic Anomaly (SAA).

Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review

Section 11a: Error Rate Calculations - Appendix

Charge Collection Fundamentals:
The Importance of Diffusion

Larry Edmonds

The First Step After an Ion Hits a DR

After an ion hits a reversed-biased pn junction depletion region (DR), the first step is a DR collapse.

- Some of the liberated carriers are rearranged by the strong electric field in the DR until the formerly unshielded impurity (doping) ions become shielded.
- What was formerly a space charge region (the pre-hit DR) is now quasi-neutral, i.e., the DR is essentially removed.
- Only a small fraction of the liberated carriers are needed to do this. Nearly all of the initial track is intact and in a quasi-neutral region.

2

The First Step After an Ion Hits a DR (cont.)

The collapse stage is effectively instantaneous from the point of view of charge collection at the device contacts.

- The rearrangement of carriers in the device interior is so fast that it is accompanied by very little charge collection at the device contacts.
- The significance of the collapse stage is to set up the initial conditions for the recovery stage that follows

3

The Recovery Stage

Nearly all charge collection at the device contacts is during the recovery stage.

At the start of the recovery stage, the DR width is almost zero, so essentially all of the track is outside the DR (in the quasi-neutral region).

Carriers in the region formerly occupied by the pre-hit DR are not "promptly" collected because they are outside the post-hit DR.

As recovery progresses, the DR boundary (DRB) gradually moves deeper into the device interior as the DR gradually regains its original width.

4

A Low-Order Approximation for Charge Collection

A particular approximation for charge collection has been called "low-order" because it ignores DRB motion.

The strong electric field in the DR prevents majority carriers from entering it.

- Under static conditions (no DRB motion), this implies that there is zero majority-carrier current in the quasi-neutral region near the DRB.
- Therefore, the potential distribution in the quasi-neutral region becomes whatever it must be to make the majority-carrier drift current balance the majority-carrier diffusion current (the existence of a potential distribution in the quasi-neutral region has been called "funneling").

5

A Low-Order Approximation for Charge Collection (cont.)

Ion hits produce high-density conditions (the carrier density greatly exceeds the doping density).

- Under high-density conditions, the electron and hole densities have nearly equal values and gradients in the quasi-neutral region.
- Therefore, majority-carrier drift being equal to majority-carrier diffusion near the DRB implies that minority-carrier drift equals minority-carrier diffusion near the DRB.
- But the minority-carrier currents add to instead of subtract from each other, so half of the total current is minority-carrier drift, and the other half is minority-carrier diffusion.
- Stated another way, the current is twice the minority-carrier diffusion current.

6

A Low-Order Approximation for Charge Collection (cont.)

To the extent that the low-order approximation applies, the current is twice the minority-carrier diffusion current [1],[2].

DRB motion upsets this condition and is one source of error in the low-order approximation.

- [1] L.D. Edmonds, "Charge Collection from Ion Tracks in Simple EPI Diodes," *IEEE Trans. Nucl. Sci.*, vol. 44, no. 3, pp. 1448-1463, June 1997.
 [2] L.D. Edmonds, "Electric Currents Through Ion Tracks in Silicon Devices," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 3153-3164, Dec. 1998.

7

Calculating the Diffusion Current

The diffusion current is calculated from the minority-carrier diffusion coefficient together with the gradient of the carrier density.

The gradient is calculated by solving an equation together with boundary conditions.

The equation describing the carrier density (not flow, but density) is the ambipolar diffusion equation.

8

Calculating the Diffusion Current (cont.)

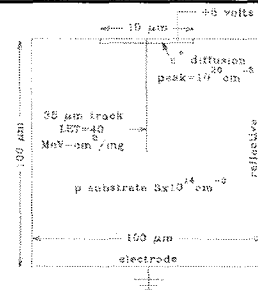
Boundary conditions are from another approximation.

- Although high-density conditions apply at the DRB, the carrier density there is still much less than elsewhere on the track.
- Therefore, an approximation treats the DRB as a sink, i.e., the carrier density there is approximated as zero for the purpose of estimating the gradient from the diffusion equation.
- This is another source of error in the low-order approximation.

9

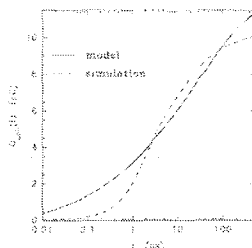
Comparison with a Simulation Result

A simple diode was simulated: a device with rotational symmetry.



10

Comparison with a Simulation Result (cont.)



Comparison of collected charge calculated from the low-order approximation to the simulation prediction.

11

Comparison with a Simulation Result (cont.)

For t less than 2 ns, the low-order approximation predicts too much current.

- The assumed sink-like boundary condition is a bad approximation at very early times.
- The over-estimation in the current persists for less than two-tenths of a nanosecond, but the collected charge is cumulative, so its error persists for a longer time.

12

Comparison with a Simulation Result (cont.)

Then the curves come together.

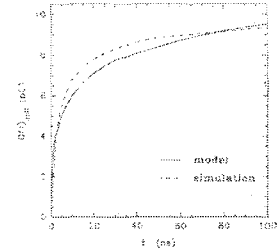
- DRB motion enhances the actual current, but is not included in the model, so the actual collected charge catches up to the model prediction at about 2 ns.
- The curves then stay fairly close together until 100 ns.

The curves diverge again after 100 ns.

- The model assumes high-density conditions for all t , which is incorrect at very large t .
- Most of the charge that ever will be collected was collected during the first one-hundred ns, so the erroneous assumption produced only a moderate error in the predicted collected charge.

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Comparison with a Simulation Result (cont.)



If the time scale of interest is measured in nanoseconds up to 100 ns, the agreement can be made to look better by using a linear time axis

14

Comparison with a Simulation Result (cont.)

- If Fig. 3 adequately represents the time scale of interest, then the low-order approximation, which is a diffusion calculation, did a pretty good job.
- For other time scales that might be of interest, the diffusion calculation predicted too much current.
- While erroneous assumptions can make the calculated collected charge from diffusion too large, it is never negligible compared to the actual collected charge.
- Diffusion is always important.

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Radiation Evaluation of the PowerPC 750 Microprocessor

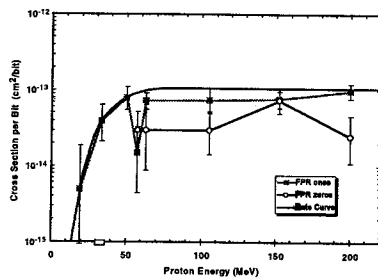
External Peer Review
Section 12: Error Rate Results
Gary Swift

Outline

- Introductory Remarks
- Model Environments for REE
- How Rates Are Calculated
- **Rate Results**
- Conclusions

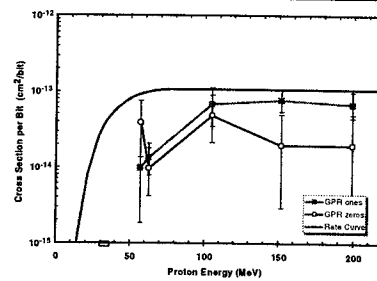
2

Proton Model Fit



3

Proton Model Fit (cont.)



4

Approach Used for Rate Calculations

Modified "RPP" Model

- Assumes "cosine law" applies to angles of 70°
- No explicit assumption of collection depth
- Charge at more extreme angles generally "shared" with other nodes

Power PC750 Has Shallow Epitaxial Region

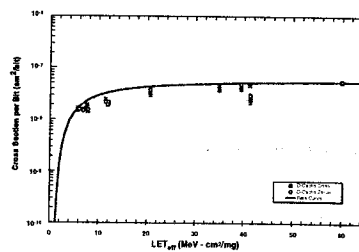
- Reduces charge collection from remote regions
- Also reduces importance of charge diffusion at later times

Other Devices May Have Thicker Charge Collection Regions

- Most advanced commercial memories use bulk substrates
- Complicates charge collection issue and assumptions

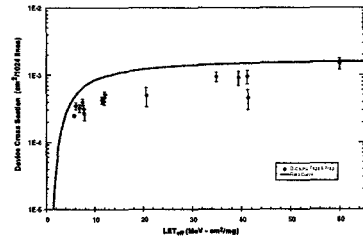
5

Heavy Ion Model Fit



6

Heavy Ion Model Fit (cont.)



7

Processor Error Rates for Registers

Space Environment	Errors per bit-day
Interplanetary Space	
Solar minimum GCR	9.4E-7
Solar maximum GCR	2.3E-7
Flare (100 mil shield)	3.5E-4
Martian Surface	5.5E-8

8

Processor Error Rates for Registers

Space Environment	Errors per bit-day
Earth Orbiter (600 km, 28 degree)	
GCR	1.5E-8
Trapped Protons	5.7E-7
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	2.4E-7
Solar maximum GCR	7.2E-8
Trapped Protons	2.7E-7
Flare (100 mil shield)	5.8E-5

9

Processor Error Rates for Registers

Space Environment	Errors per bit-day
Interplanetary Space Flare (protons + ions)	
Shield Thickness (Al equiv.)	
60 mil	2.0E-3
100 mil	3.5E-4
250 mil	1.9E-4
Earth Orbiter (600 km, 98 degree)	
Shield Thickness (Al equiv.)	
60 mil	5.0E-4
100 mil	5.8E-5
250 mil	3.5E-5

10

Peak Rates for Registers

Space Environment	Ratio Peak-to-Average Daily Rate
Interplanetary Space	
Flare (100 mil shield)	4.6
Earth Orbiter (600 km, 28 degree)	
GCR	1.0
Trapped Protons	32
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	3.9
Solar maximum GCR	3.2
Trapped Protons	67
Flare (100 mil shield)	28

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Processor Error Rates for Data Cache

Space Environment	Errors per bit-day
Interplanetary Space Flare (protons + ions)	
Shield Thickness (Al equiv.)	
60 mil	1.9E-3
100 mil	3.8E-4
250 mil	1.8E-4
Earth Orbiter (600 km, 98 degree)	
Shield Thickness (Al equiv.)	
60 mil	4.8E-4
100 mil	8.0E-5
250 mil	3.5E-5

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Data Cache Error Rates

Space Environment	Errors per bit-day
Interplanetary Space	
Solar minimum GCR	7.0E-7
Solar maximum GCR	1.9E-7
Flare (100 mil shield)	3.8E-4
Martian Surface	5.0E-8

13

Data Cache Error Rates

Space Environment	Errors per bit-day
Earth Orbiter (600 km, 28 degree)	
GCR	1.7E-8
Trapped Protons	3.7E-7
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	1.9E-7
Solar maximum GCR	6.4E-8
Trapped Protons	1.8E-7
Flare (100 mil shield)	8.0E-5

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Data Cache Peak Error Rates

Space Environment	Ratio Peak-to-Average Daily Rate
Interplanetary Space	
Flare (100 mil shield)	4.2
Earth Orbiter (600 km, 28 degree)	
GCR	1.0
Trapped Protons	30
Earth Orbiter (600 km, 98 degree)	
Solar minimum GCR	3.7
Solar maximum GCR	3.0
Trapped Protons	61
Flare (100 mil shield)	20

15

Conclusions Space Error Rates for PC750 at Chip Level

Deep Space (Galactic Cosmic Rays)

- Errors in registers and cache approximately every other day
 - Without cache, errors approximately every month
 - However, turning off cache adversely affects performance
- Crashes may also occur (can't quantify well at this stage)

Solar Flare

- Error rates approximately 400 times higher
- Several hundred errors during "design-case" flare (24 hours)

Earth Orbiting Applications

- Daily average rate higher, dominated by trapped protons
- Solar flare increases error rate by factor of 40

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Conclusions

- Proton rates tend to dominate heavy ion rates for environments with significant proton components:

- Earth Orbit (due to trapped protons)
- Large Flares

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Radiation Evaluation of the PowerPC 750 Microprocessor

External Peer Review
Section 13: Plans & Conclusions
Gary Swift

Recent Testing

Tests of TLB's (page table cache)

- Low energy proton at UC Davis
- Heavy ion testing at Texas A&M

Tests of G4 (MPC7400)

- Low energy proton at UC Davis
- Heavy ion testing at Texas A&M

Tests of IBM PPC750

- Heavy ion testing at Texas A&M

Tests of L2 Tags & Flag

- Low energy proton at UC Davis
- Heavy ion testing at Texas A&M

2

Next Steps

Complete Motorola XPC750 Tests

- High energy protons of TLB's and L2 tags and flag
- Fill in heavy ion LET "holes" in data, especially very low LET
- More tests of L1 instruction cache
- Develop branch table cache test (?)

Associated Circuitry

- Complete three manufacturers' cache SRAMs
- Begin testing a PCI bridge chip
 - Socketting yellowknife has not worked
 - Must build custom test card

Complete tests of IBM PPC750 and Motorola G4

3

Next Steps (cont.)

More dynamic operations testing (using FPU test)

- Find LET threshold
- Look for scaling effects using G4
- Look for scaling effects using smaller 750

4

Further Steps

Conduct a major campaign investigating hangs

- Developing custom hardware to halt processor immediately
- Capturing device pin states with logic analyzer
 - Any illegal states ??
 - When do errors (and what types) propagate to the pins?
- Can more types of hangs be caught ?
 - More trapping possible ?
 - At least, identify and classify more types

Continue to push toward fully understood "application testing"

- Can error model be validated this way?
- Error detection in "new" programs possible?

Test scaled versions of PowerPC family for comparison

5

Known Problem Areas

Need tests of angular response to heavy ions

- Experimental data is critical to upset rates (validate or invalidate that R=5 for RPP aspect ratio)

Need to analyze data for:

- Hang information and ballpark rates
- Multiple upset bits from single events
- Different register responses, especially within SPR type

Need to measure lower LET cross sections

- Upset rate is particularly sensitive to our assumptions here

Could investigate 60 MeV proton discrepancy

6

Conclusion

Will complete register and cache and associated chip characterization of the Motorola PowerPC 750 soon.

Verification that major important effects are now known should be attempted using well-analyzed "application-like" benchmarks.

Much has been accomplished, much remains to be done.

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